

Digital baseband algorithmic and architectural solutions to master complexity

LIANG LIU, DEPT. OF ELECTRICAL AND INFORMATION TECHNOLOGY, LUND UNIVERSITY



Massive number of antenna elements

... Leads to

Increased MIMO processing complexity

More antenna tranceiver units

More data to stored and send between transceivers and baseband processing units



- 1. What can be done to make MIMO processing more computational efficient?
- 2. How can digital baseband processing relax the requirement on analog compoments?
- 3. How can we handle the massive data storage?



Efficient precoding and detection architecture and circuitries



Distributed architecture for MRT



Hybrid architecture for ZF precoding





DSP assistants the use of low-cost analog components



Enable low-cost analog components



Reducing PA dynamic range with antenna reservation (concept)



Reducing PA dynamic range with antenna reservation (performance)



Implementation: Reserving 20 of 100 antennas with 10 users reduces PA back-off by **3-4 dB** at a cost of only **15%** increase in precoding complexity (comparing to QRD-based ZF precoder)



Compensating IQ-imbalance (system model)



Compensating IQ-imbalance (scheme)



ltem	Value
Process	ST 28nm
Power	0.61mW
Latency	2clk @ 200MHz
Gate count	24k

Large diagonal elements. Can be efficiently implemented as a Jacobi iterative solver



One instance per antenna

Compensating IQ-imbalance (result)



Simulated IQ imbalance with mean value 6% amplitude and 6 degree phase imbalance (random on antennas)



Reciprocity calibration (system model)

 Channel reciprocity is used to realize efficient TDD Massive MIMO





Reciprocity calibration (scheme)

- Calibrate by referering to the same base-station antenna
 - Calibration within base-station
 - Use antenna coupling for the estimation



Calibration between

Reciprocity calibration (processing distribution)



Parallel memory for channel matrix storage



Memory subsystem in Massive MIMO

High capacity and throughput

□ Storage v.s. processing (150 subcarriers)

Channel matrix Memory	QRD-based ZF precoder
0.28mm ²	0.13mm ²

- Multiple access patterns
 - Column wise: *H*^H*H*
 - Row wise: *Hy*
 - Diagonal wise: *H*^H*H*+α*I*
- Adjustable operand matrix size





Hardware implementation of a 16-bank parallel memory

- Capacity 128kB: 15 subcarriers of 128×16 MIMO system
- Row/Column/Diagonal (16 elements) access in one clock cycle
- > 0.28 mm² in ST 28nm technique
- ≻64 GB/s Throughput@1 GHz Frequency
- Power consumption
 - □ 197mW @write
 - □ 246mW @fetch





Exploiting the sparsity in massive MIMO channel



Distribution of angle of arrival signals at base station (Real measured result with linear array of 128 antenna elements)



FFT-based channel data compression





Conclusions

- Efficient MIMO processing using massive MIMO properties
- DSP enables low-cost analog components
- Memory is crucial to achieve energy- and area- efficient

baseband processing

