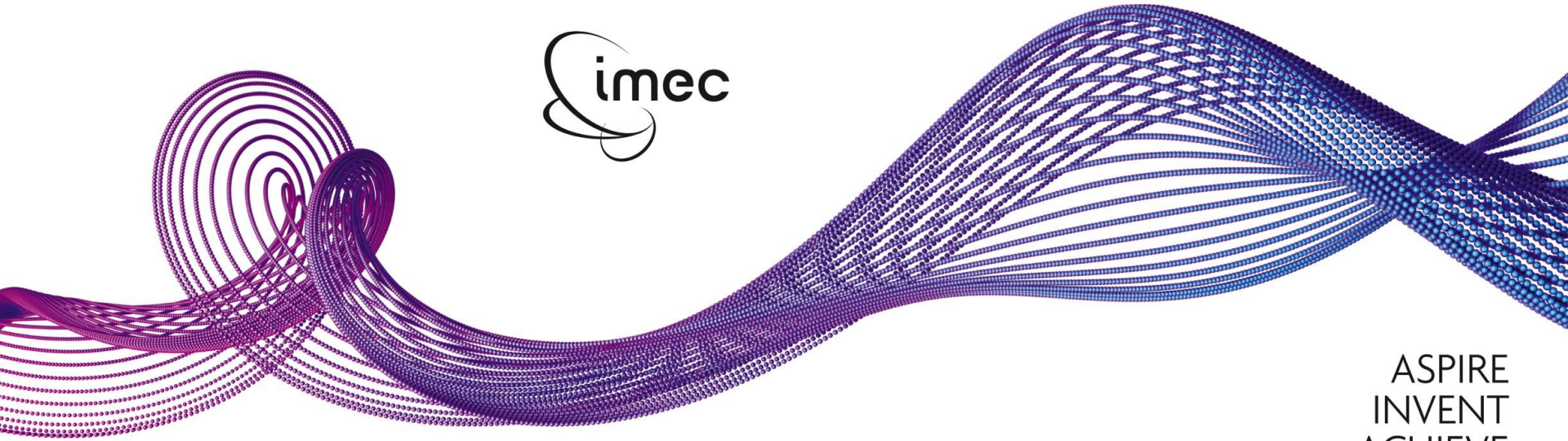
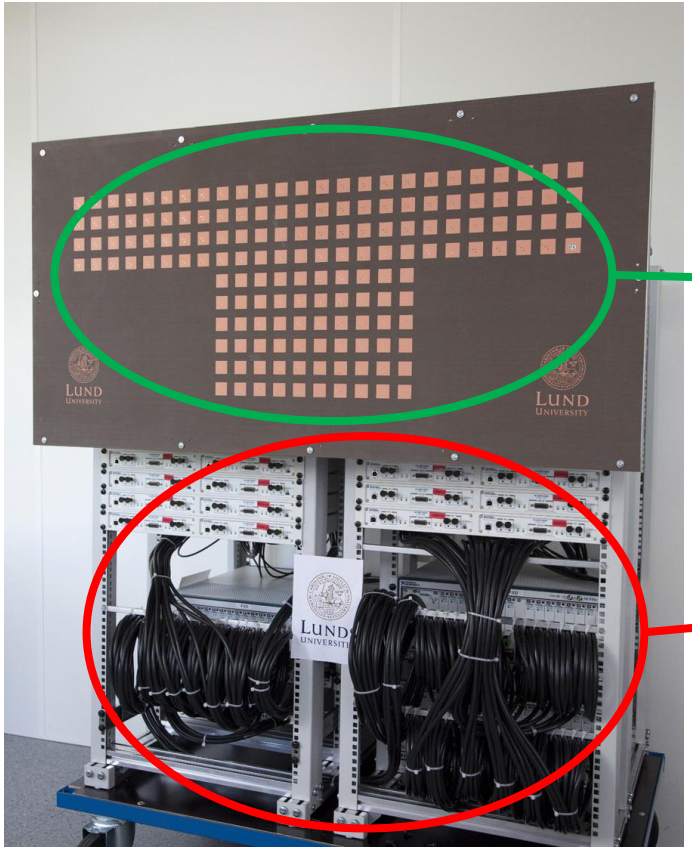
LOW-POWER ADCS FOR MASSIVE MIMO SYSTEMS

JAN CRANINCKX



ASPIRE
INVENT
ACHIEVE

MASSIVE HARDWARE NEEDS FOR MASSIVE MIMO



High data rates and many users enabled by a massive amount of antennas

Some extra hardware needed...

ENERGY-EFFICIENT WIRELESS ADCS

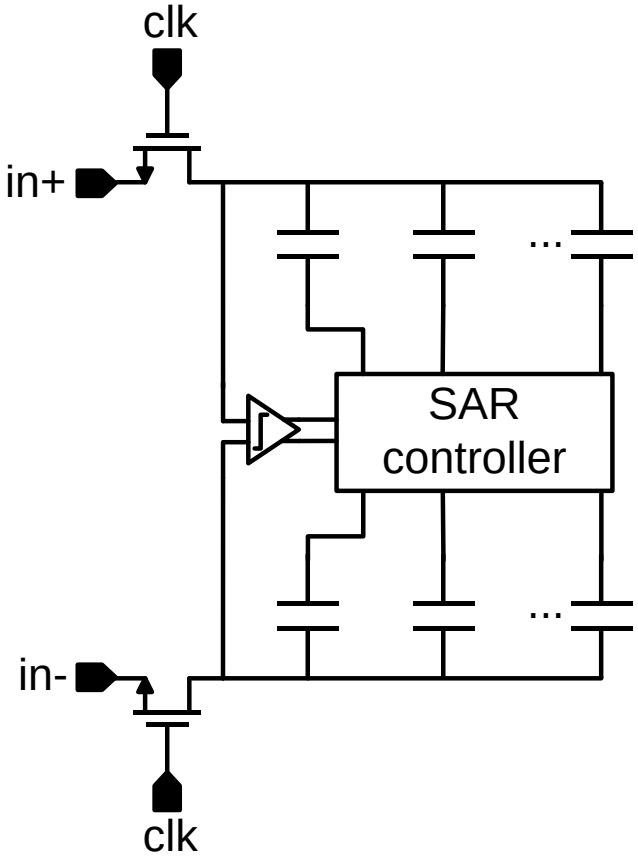
- Performance requirements
  - >10 ENOB
  - 100's MS/s
  - Low power consumption (mW)

- Architecture choice
  - SAR: successive approximation
  - N comparisons needed for an N-bit ADC
  - Nanoscale CMOS offers enough speed to reach required sampling rates

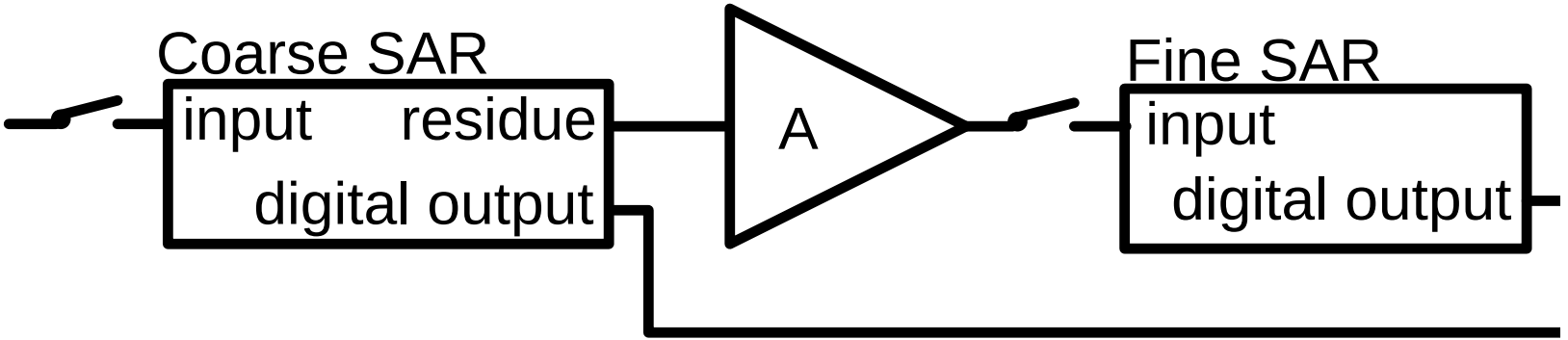
OUTLINE

- ADC Architecture
  - Channel implementation
- Calibration methods
- Implementations and measurements
- Conclusions

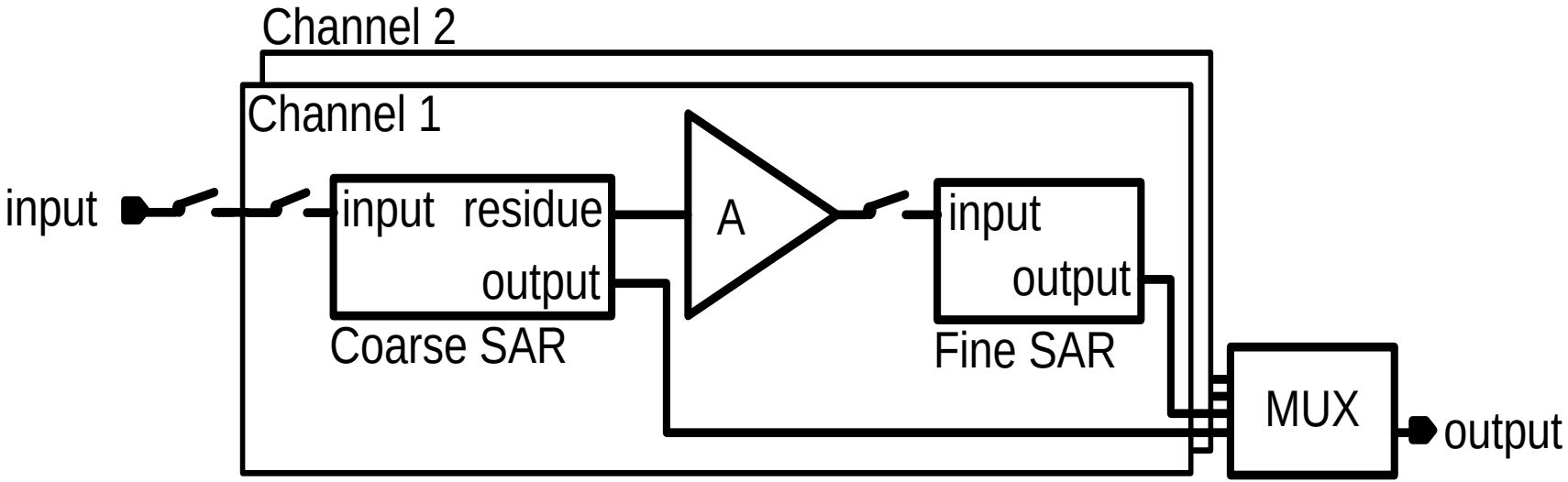
START FROM SAR ADC FOR EFFICIENCY



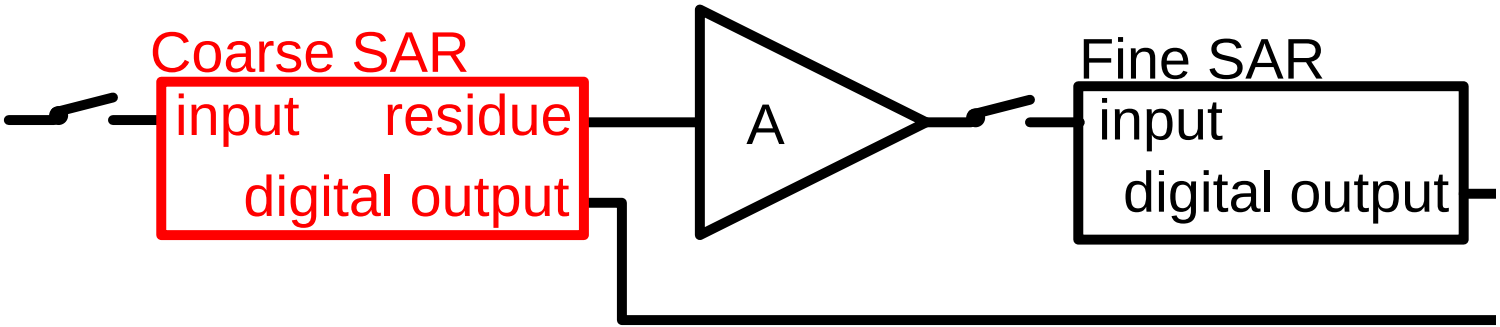
PIPELINE FOR SPEED



INTERLEAVE FOR MORE SPEED



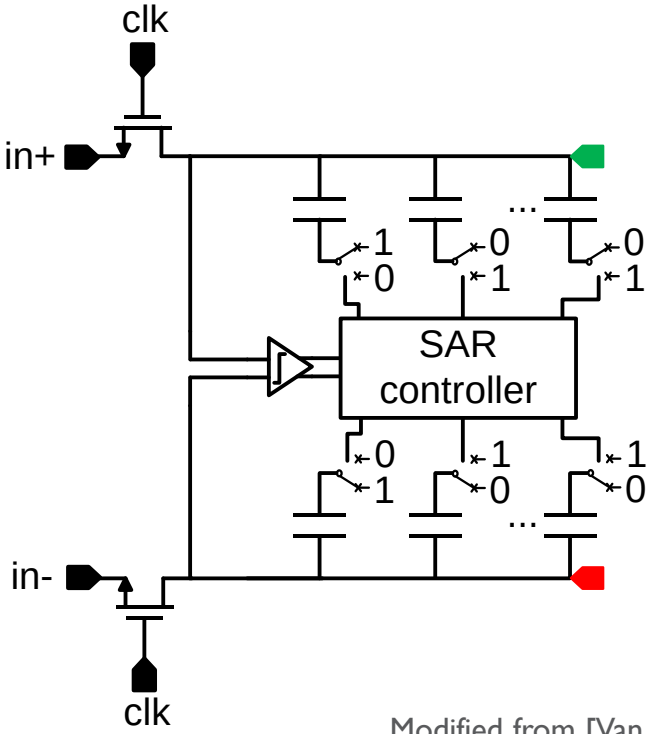
ADC CHANNEL (1):
COARSE SAR SAMPLES AND GENERATES RESIDUE

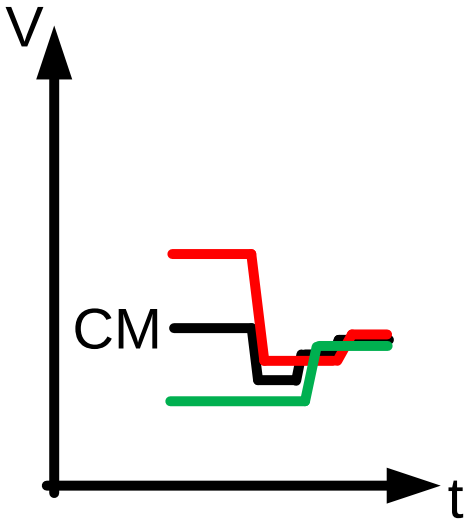


- 6 cycle binary scaled SAR
- 1b redundancy in backend
  - robust to comparator errors

SINGLE-ENDED DAC SWITCHING SCHEME

FOR LOW ENERGY, GOOD SPEED

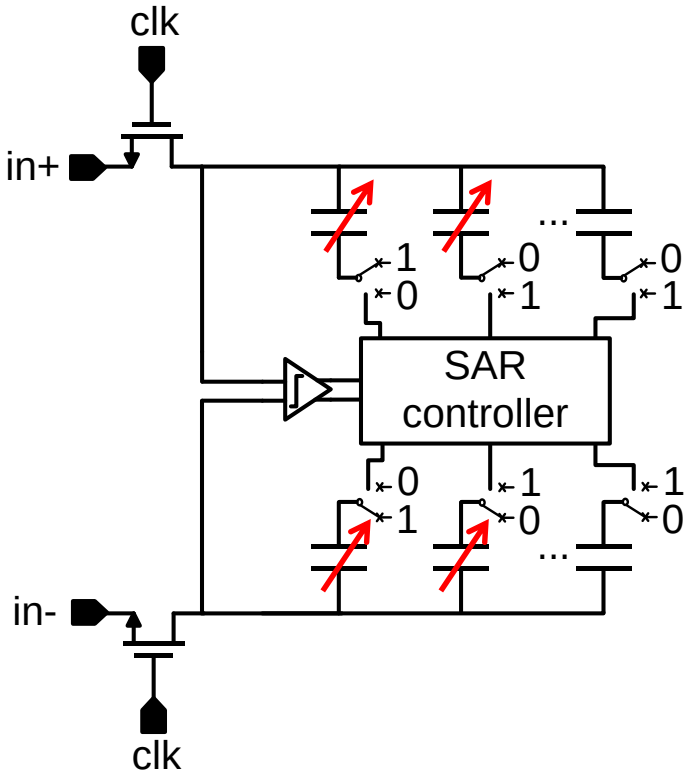




Modified from [Van der Plas ISSCC 2008] and [Liu VLSI 2009]

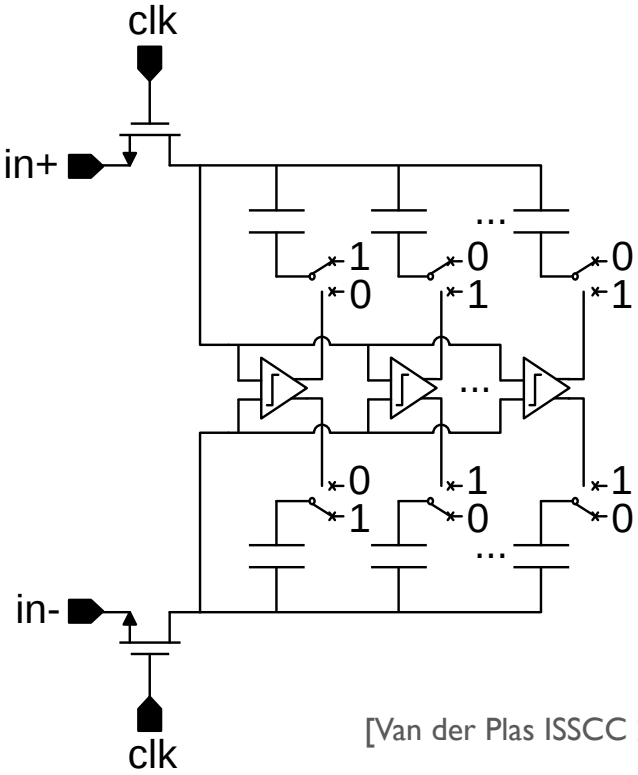
DAC LINEARITY IS CRITICAL

- Total capacitance = 3.5 pF
  - Approx. 13b noise
- Calibration for 3 MSBs
  - Programmable capacitance
  - Digital coefficients binary scaled
  - LSBs sufficiently matched



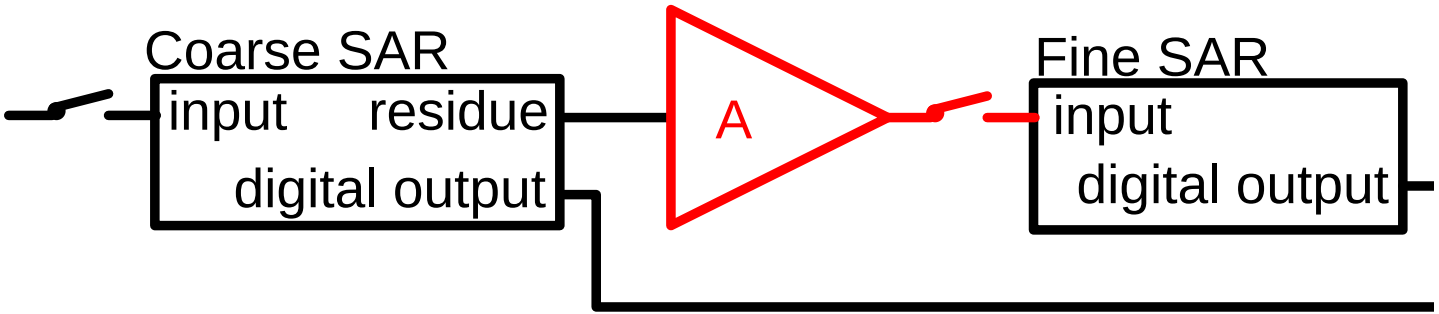
CONTROLLER REPLACED BY COMPARATORS + DELAYS

- Each comparator activated at specific common-mode
  - Calibrate offset at this common-mode
- Reduces power consumption



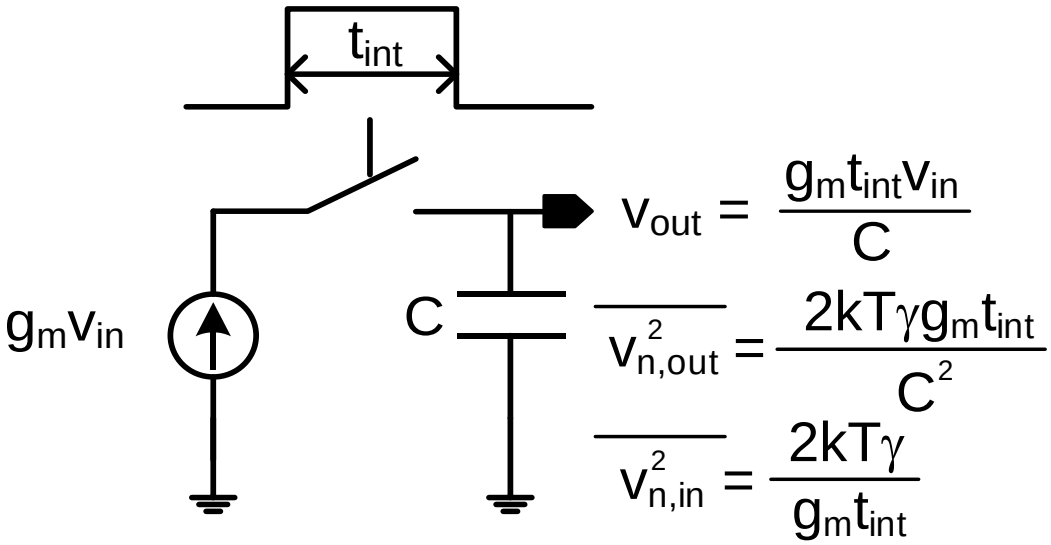
[Van der Plas ISSCC 2008]

ADC CHANNEL (2):
DYNAMIC RESIDUE AMPLIFICATION



- Amplify and sample residue
- Small output swing ➔ relaxed linearity
- Uncertain gain ➔ match coarse SAR LSB to fine SAR MSB in calibration
- Fast amplification with low noise at low power

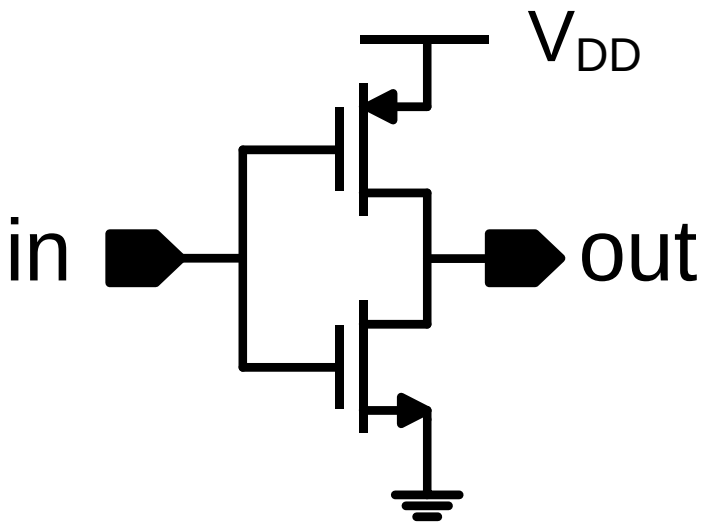
DYNAMIC AMPLIFIER = INTEGRATION DURING CERTAIN TIME



$$E = V_{dd} \cdot I_D \cdot t_{int}$$

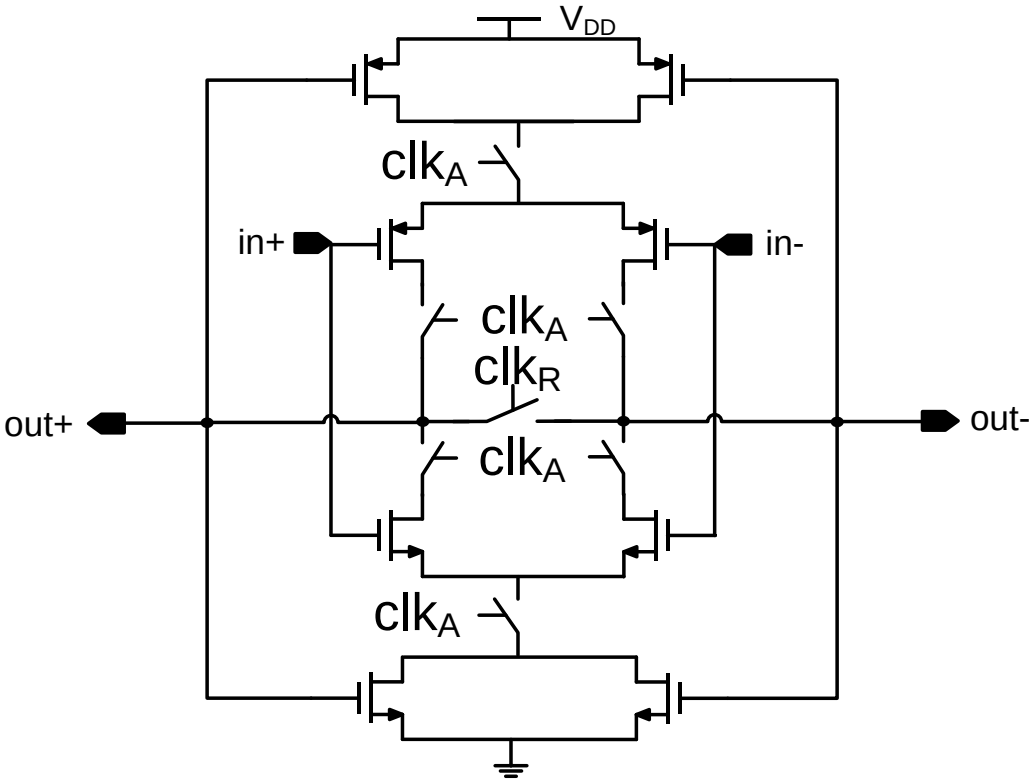
Low noise requires high g_m or long integration time

INVERTER IS GOOD TRANSCONDUCTOR

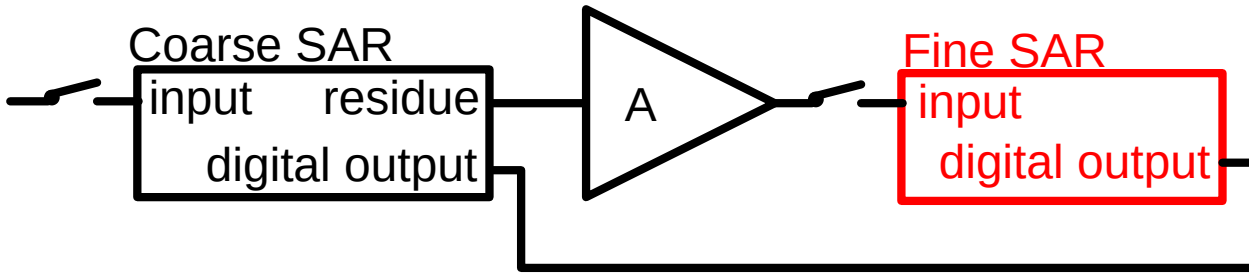


- PMOS and NMOS contribute gm
- Shared bias current➔ efficiency

DIFFERENTIALLY, COMMON MODE FEEDBACK, START/END INTEGRATION

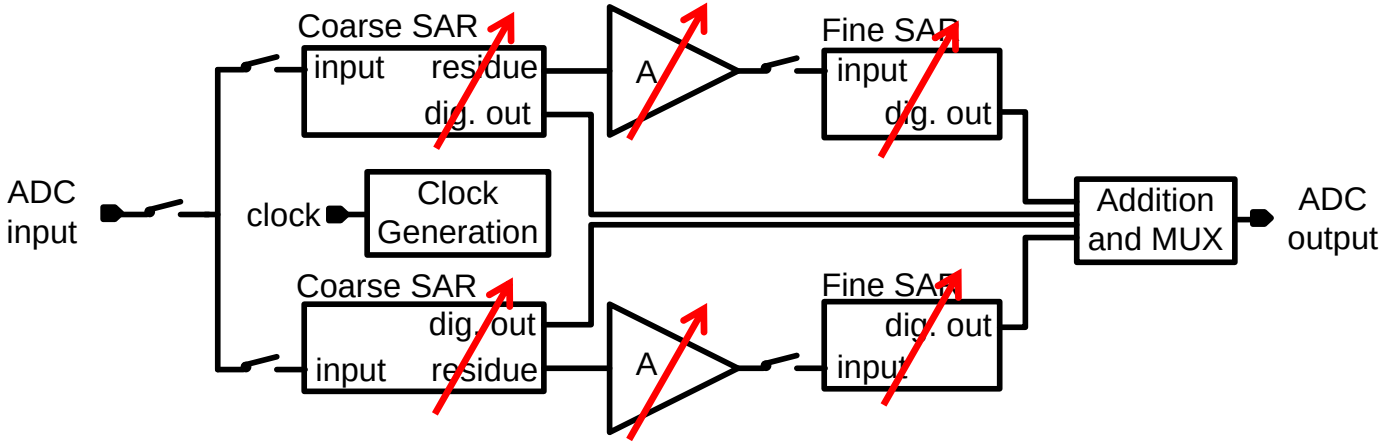


ADC CHANNEL (3):
FINE SAR QUANTIZES RESIDUE



- 8 cycle binary SAR w/ intermediate noise
  - 400 μV r.m.s.
- 2 cycle binary SAR w/ low noise
  - 200 μV r.m.s.
- 1b redundancy between
- Similar implementation to coarse SAR

POWER EFFICIENCY ENABLED BY CALIBRATION



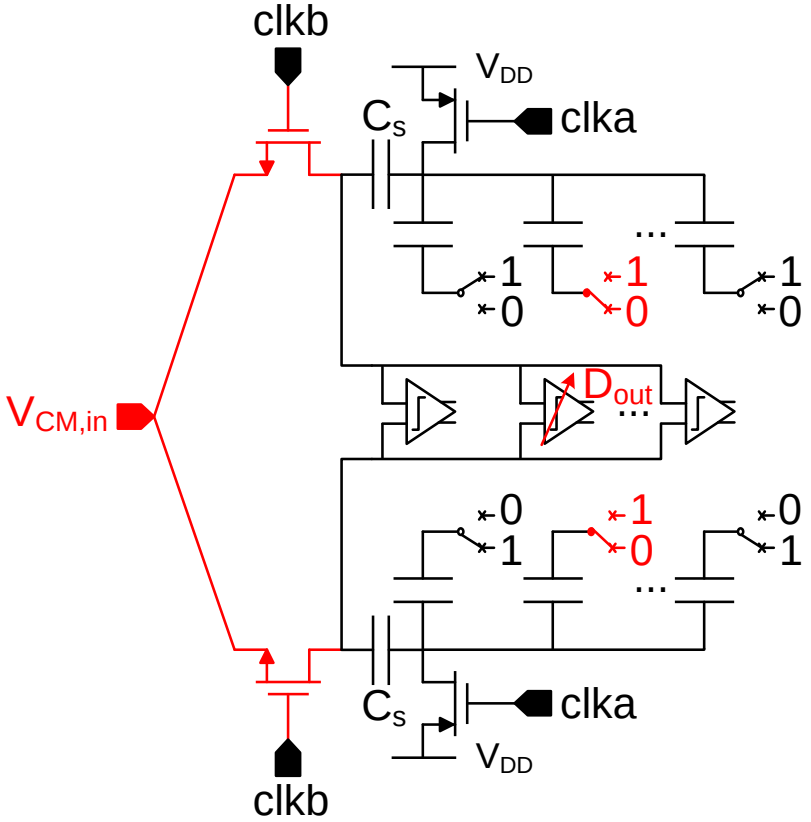
- Calibration corrects
  - DAC mismatch
  - Comparator thresholds: 6 coarse stage, 7 fine stage
  - Residue amplifier gain
  - Channel gain

COMPARATOR OFFSET CALIBRATION

OFF-LINE

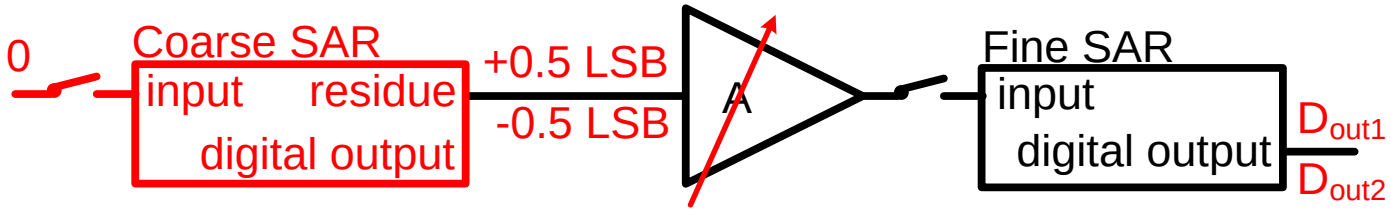
- Short ADC input
- Use DAC to generate correct common-mode
- Change comparator thresholds to average Dout = 0.5

- In second stage: Also cancels amplifier offset
- Sensitive to PVT



INTER-STAGE GAIN CALIBRATION

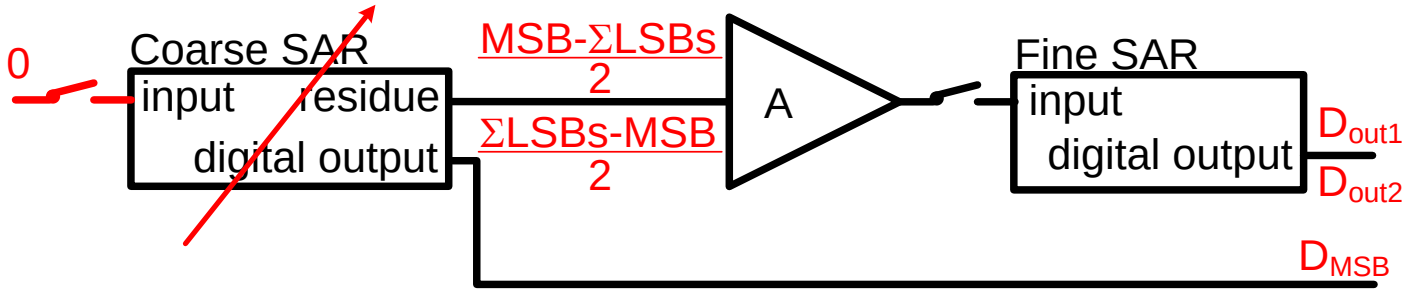
OFF-LINE



- Short ADC input
- Use coarse DAC to generate +0.5/-0.5 coarse LSB amplifier input
- Change gain to obtain Dout1-Dout2 = 1 fine MSB
- Sensitive to PVT

MSB CAPACITANCE CALIBRATION

OFF-LINE



- Short ADC input
- MSB comparator noise ➔ 2 residue values
- Use second stage to measure MSB – S(LSBs)
- Change MSB size to obtain Dout1-Dout2 = 1 fine MSB
- Insensitive to PVT

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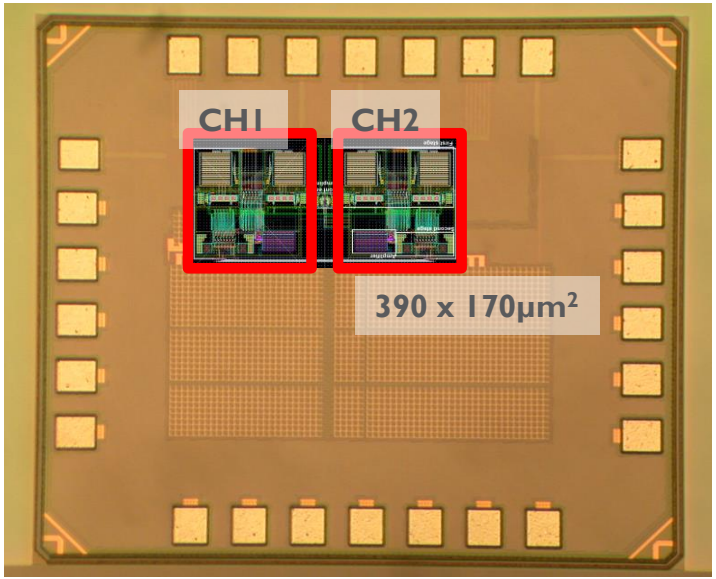
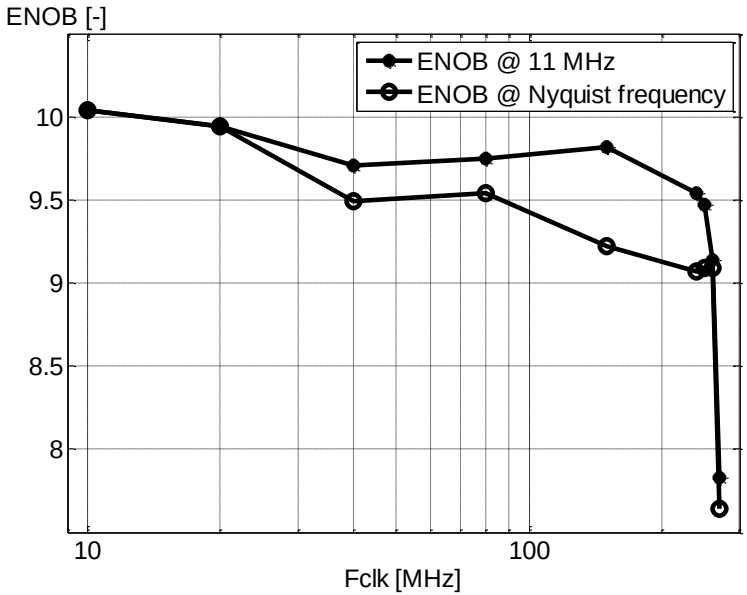
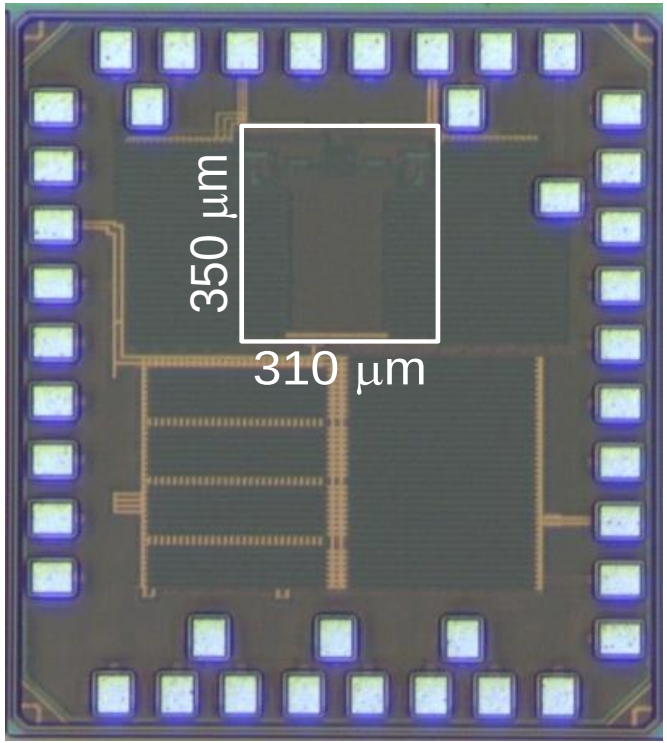
1.7mW 11b 250MS/s in 40nm

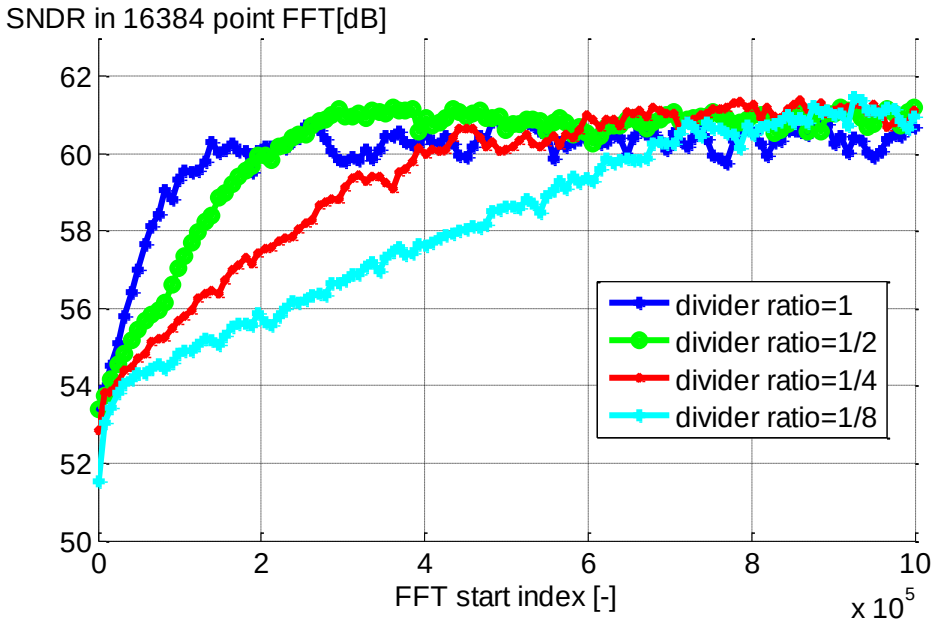




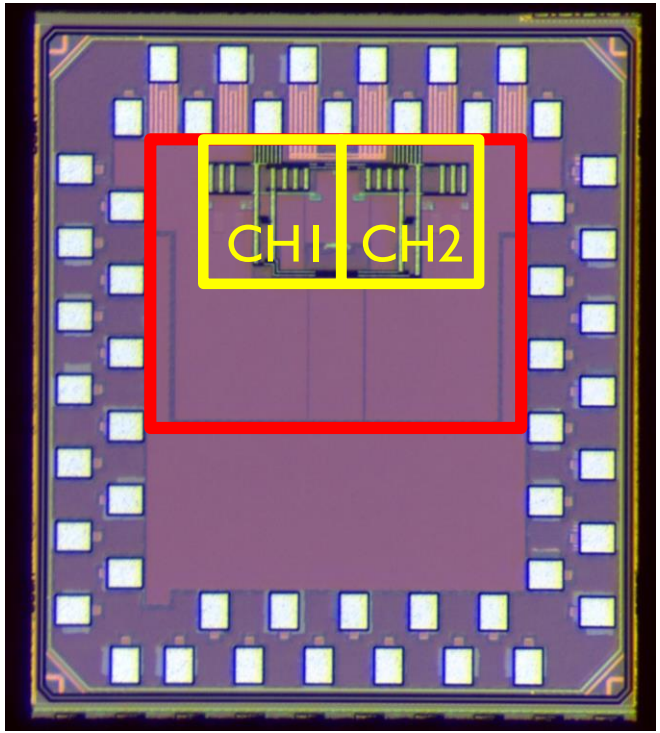
2.1mW 11b 410MS/s in 28nm

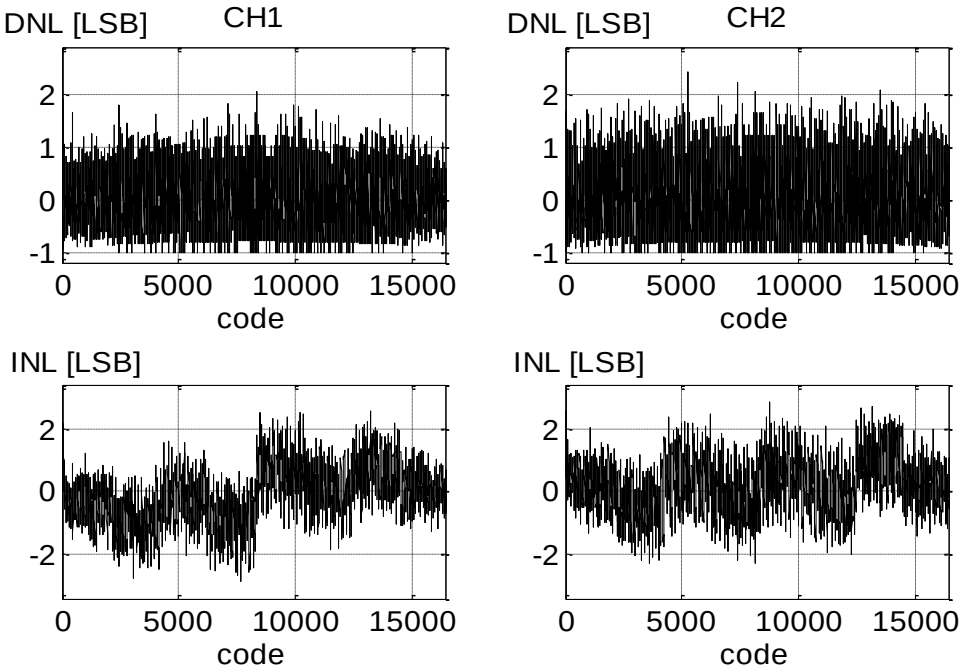
WITH BACKGROUND ON-CHIP CALIBRATION ENGINE





2.3mW 14b 200 MS/s in 28nm





CONCLUSIONS

- SAR architecture and its improvements enable power-efficient data conversion for wireless systems
  - Dynamic and asynchronous controller
  - Pipelined
  - Time-interleaved
- Nanoscale digital CMOS for SoC integration
- 1 to 2mW power consumption
  - Negligible in the overall system power

REFERENCES

- B. Verbruggen, M. Iriguchi and J. Craninckx, "A 1.7mW 11b 250MS/s 2× interleaved fully dynamic pipelined SAR ADC in 40nm digital CMOS," 2012 IEEE International Solid-State Circuits Conference, San Francisco, CA, 2012, pp. 466-468.
- B. Verbruggen, M. Iriguchi and J. Craninckx, "A 1.7 mW 11b 250 MS/s 2-Times Interleaved Fully Dynamic Pipelined SAR ADC in 40 nm Digital CMOS," in IEEE Journal of Solid-State Circuits, vol. 47, no. 12, pp. 2880-2887, Dec. 2012.
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- B. Verbruggen, K. Deguchi, B. Malki and J. Craninckx, "A 70 dB SNDR 200 MS/s 2.3 mW dynamic pipelined SAR ADC in 28nm digital CMOS," 2014 Symposium on VLSI Circuits Digest of Technical Papers, Honolulu, HI, 2014, pp. 1-2.
- B. Malki, B. Verbruggen, P. Wambacq, K. Deguchi, M. Iriguchi and J. Craninckx, "A complementary dynamic residue amplifier for a 67 dB SNDR 1.36 mW 170 MS/s pipelined SAR ADC," European Solid State Circuits Conference (ESSCIRC), ESSCIRC 2014 - 40th, Venice Lido, 2014, pp. 215-218.

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