Mixed Analog-Digital Pulse-Width Modulator for Massive-MIMO Transmitters

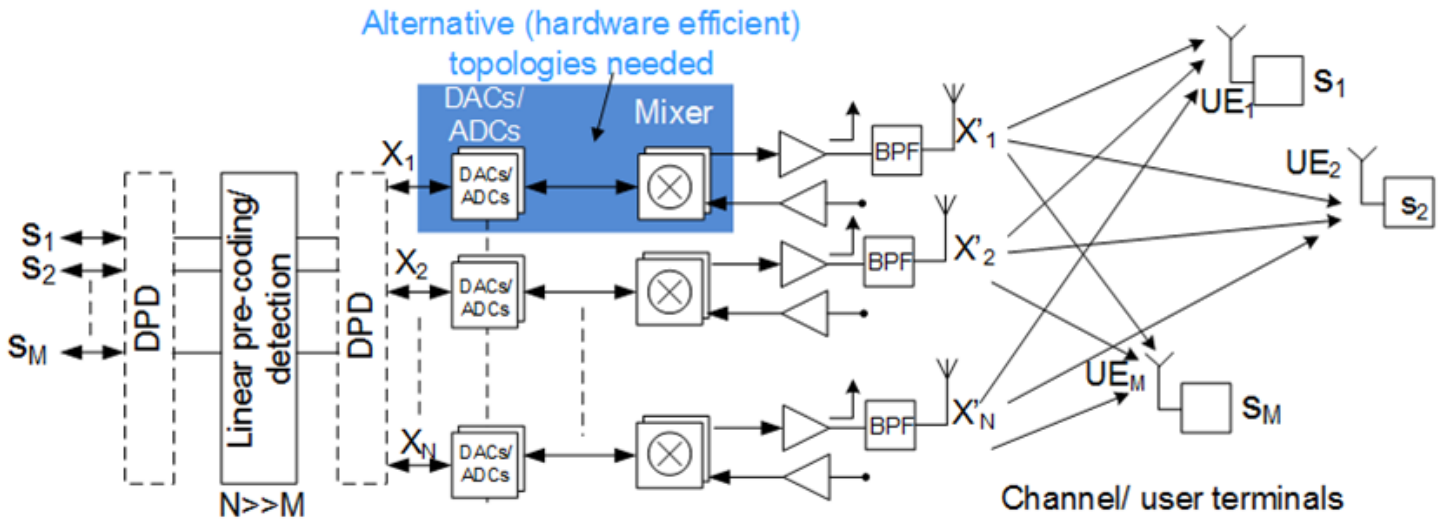
Nikolaos Alexiou
Infineon Technologies AG Austria

OUTLINE

- All-digital transmitters overview
- Digital to Time Conversion
- Proposed mixed-signal Outphasing RF Pulse-Width Modulator
- Mixed-signal co-simulation environment and simulation results
- Conclusions

- All-digital transmitters overview
- Digital to Time Conversion
- Proposed mixed-signal Outphasing RF Pulse-Width Modulator
- Mixed-signal co-simulation environment and simulation results
- Conclusions

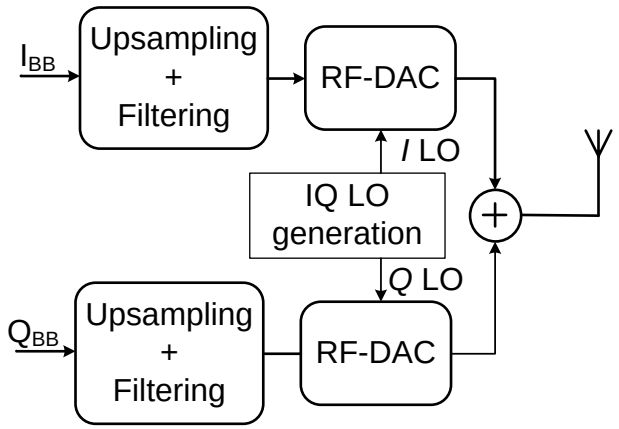
Massive MIMO block diagram



- Near linear increase of area and power consumption with array size
- Traditional analog/RF approach becomes inefficient
- Need for
  - Multi-Band / Multi-Mode
  - Wideband operation
  - Power efficiency
  - Less complexity
- Solution: All-digital transceivers
  - PWM-based digital RF transceiver
  - RF DAC - based IQ transmitter

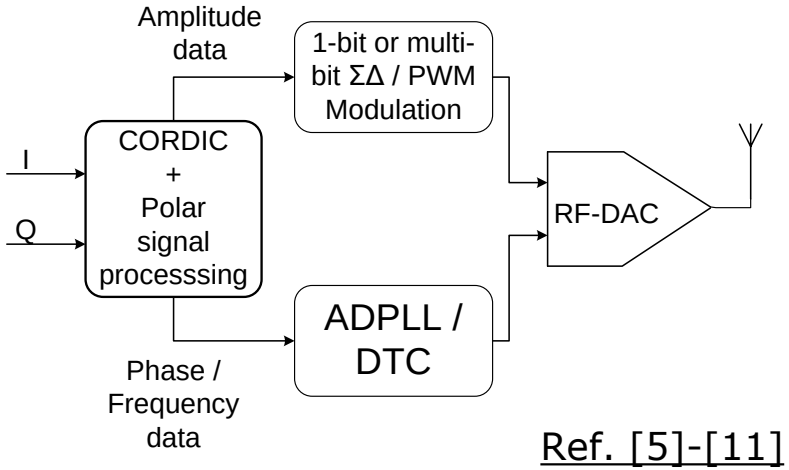
All-Digital Transmitters

IQ transmitter



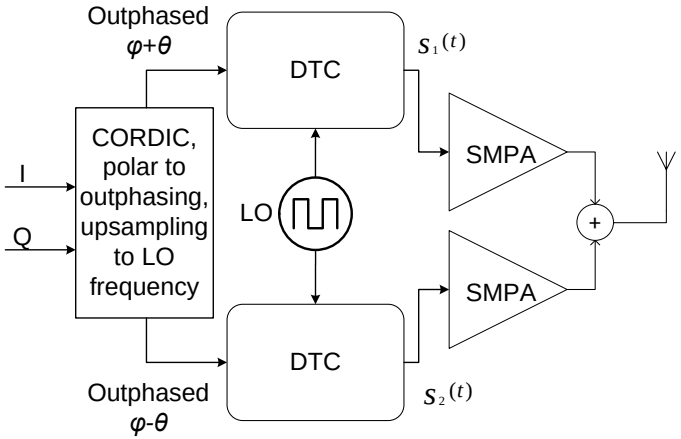
Ref. [1]-[4]

Polar transmitter



Ref. [5]-[11]

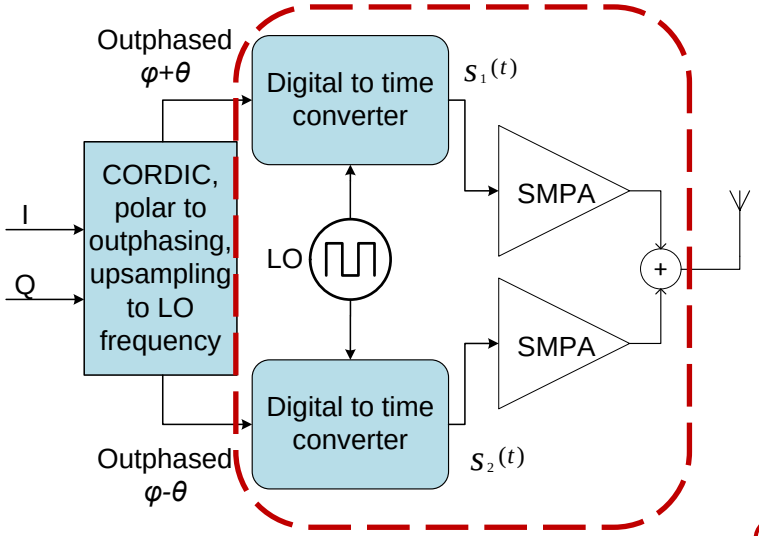
Outphasing transmitter



- Main modulation techniques
  - Direct digital to RF conversion
  - Two-point phase/frequency modulation in PLL
  - ΣΔ or Pulse Width Modulation for Amplitude modulation
  - Carrier phase modulation

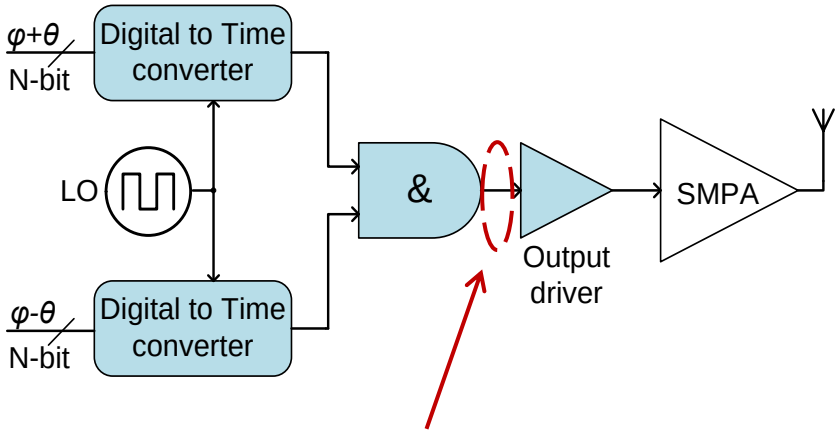
All-Digital Modulators: Outphasing Architecture

› **Traditional outphasing topology**



PWM

› **PWM based outphasing topology**



› Single-bit output for driving only one SMPA
› No power combining, no PA loading effect

› **Digital to Time Converter**
- ❑ Continuous time implementation:
  1. Phase shifting $\varphi+\theta$ / $\varphi-\theta$ using tapped delay lines (coarse time delay) and Gm-RC blocks (fine time delay) in cascade
  2. Phase Multiplexing
  3. Synchronous or Asynchronous LO phase selection

Ref. [12]-[16]

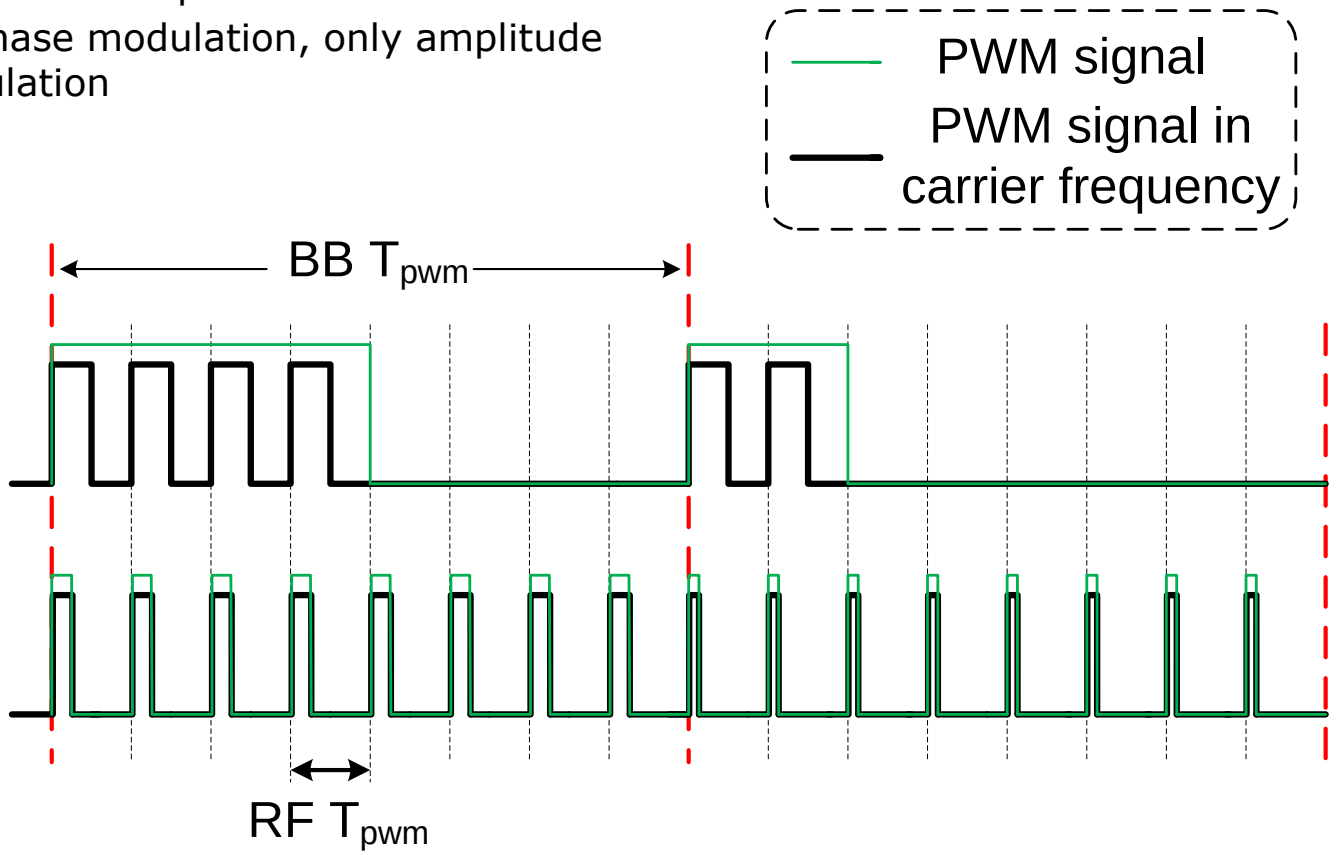
Pulse Width Modulation (time-domain)

- **Two types:**
  - Baseband PWM
  - RF PWM
- **Main difference:** Sampling frequency f_{pwm}
- **BB PWM:**
  - Bursts of phase modulated carrier pulses even for small/moderate amplitude values
  - More efficient for switching class D/E PAs
- **RF PWM:**
  - Each pulse is pulse width modulated
  - Hard to produce narrow pulses in the output
  - Pulse swallowing in PWM generation circuitry and output driver limits dynamic range

Pulse Width Modulation (time-domain)

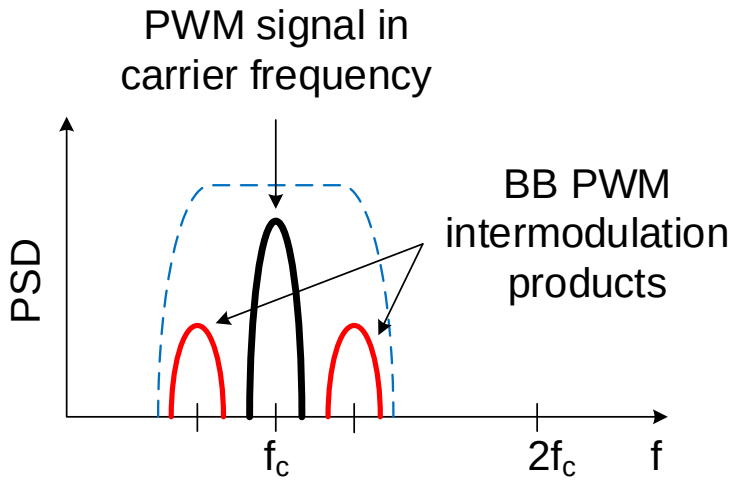
Example waveforms

- Output carrier pulses in BB and RF PWM
- No phase modulation, only amplitude modulation

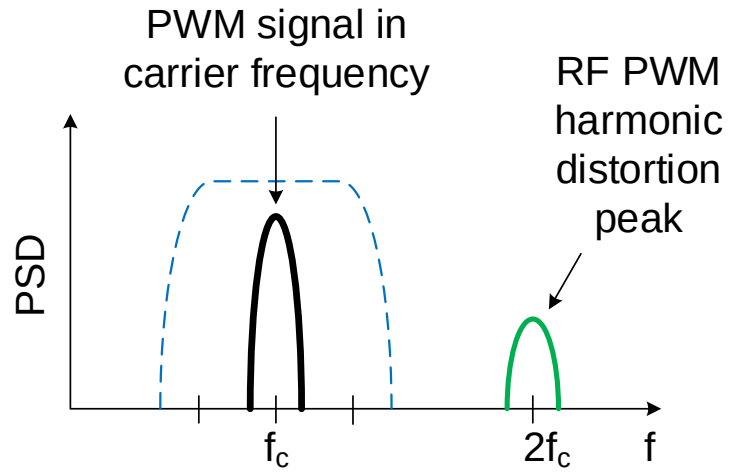


Pulse Width Modulation (frequency-domain)

- BB PWM
  - Digital mixing of PWM signal with Phase Modulated carrier.
  - Intermodulation products close to carrier.

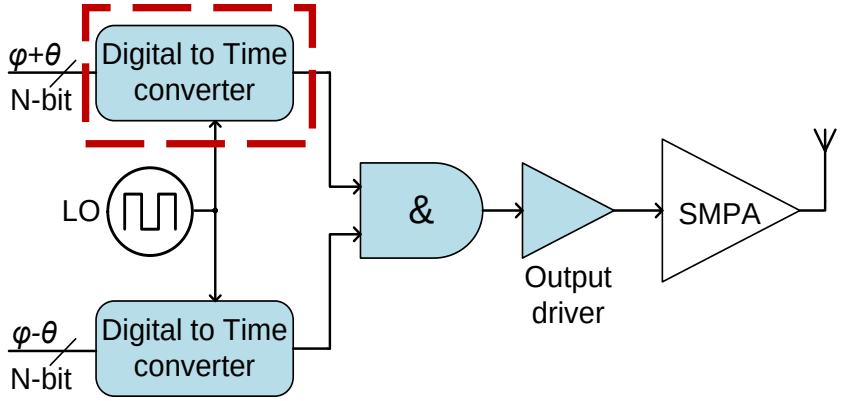


- RF PWM
  - PWM and Phase Modulation on the same pulse inside carrier period.
  - Harmonic distortion peaks @ multiples of $f_{pwm} = f_{carrier}$



- All-digital transmitters overview
- Digital to Time Conversion
  - All-Digital implementation
  - Mixed-Signal implementation
- Proposed mixed-signal Outphasing RF Pulse-Width Modulator
- Mixed-signal co-simulation environment and simulation results
- Conclusions

Digital to Time Conversion

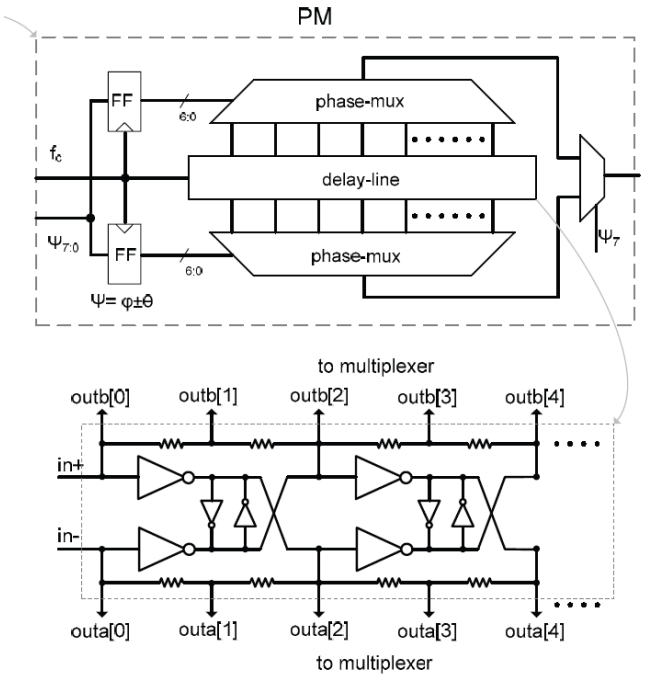


- Continuous-time
- Delay Line - based
- Two implementations
  - Digital
  - Mixed-signal

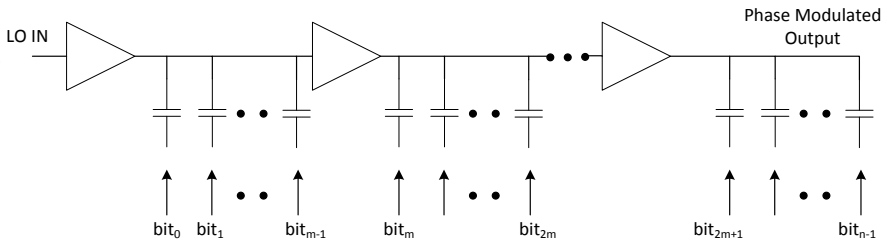
- All-digital transmitters overview
- Digital to Time Conversion
  - All-Digital implementation
  - Mixed-Signal implementation
- Proposed mixed-signal Outphasing RF Pulse-Width Modulator
- Mixed-signal co-simulation environment and simulation results
- Conclusions

Ref. [16]: Continuous-Time Digital Phase Shifting

Coarse phase shifting

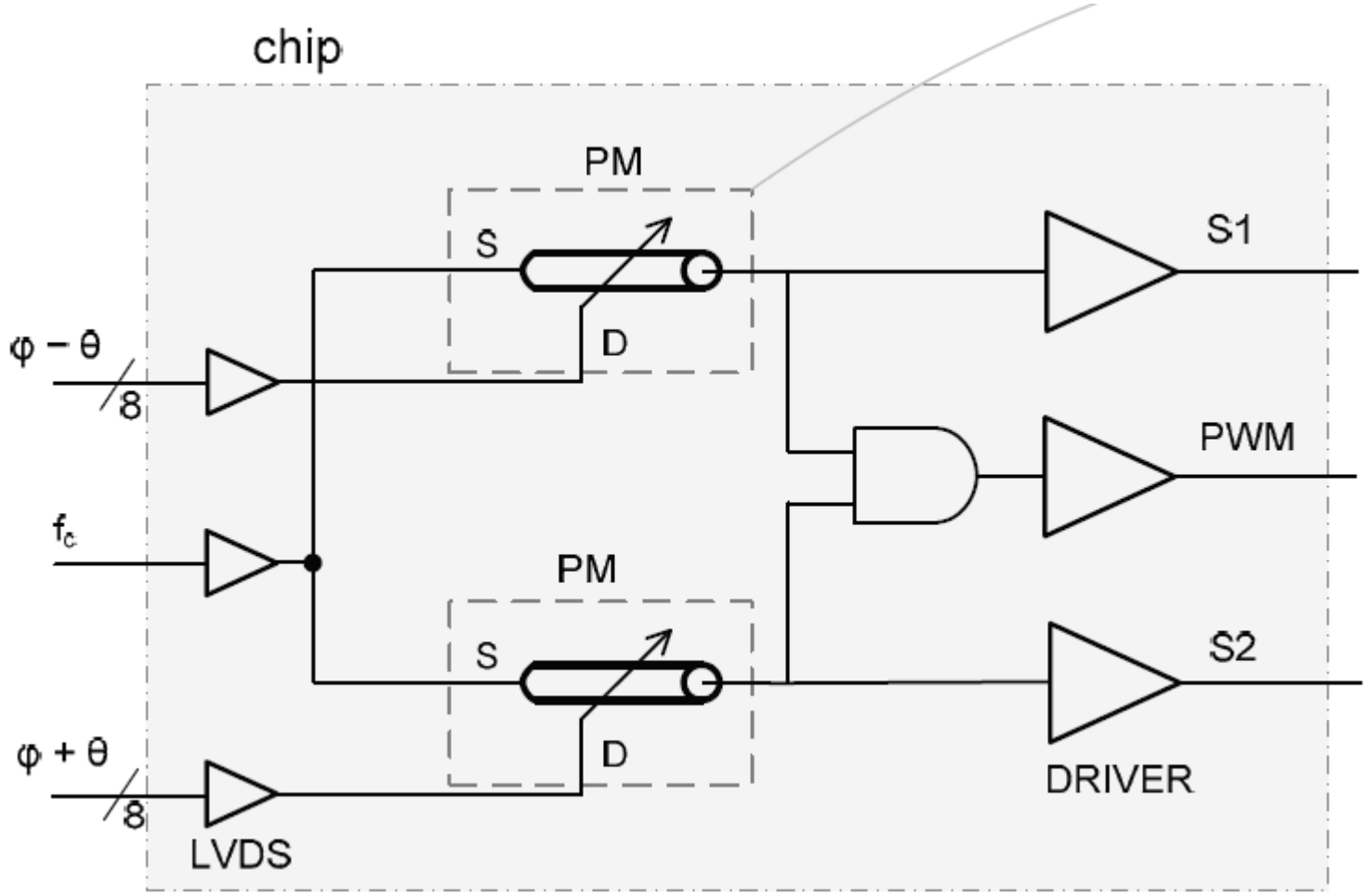


Fine phase shifting



- 8/9-bit time resolution
- For finer resolution finer-node CMOS processes must be used
- Sensitive to supply/ground noise and temperature drift
- Differential implementation

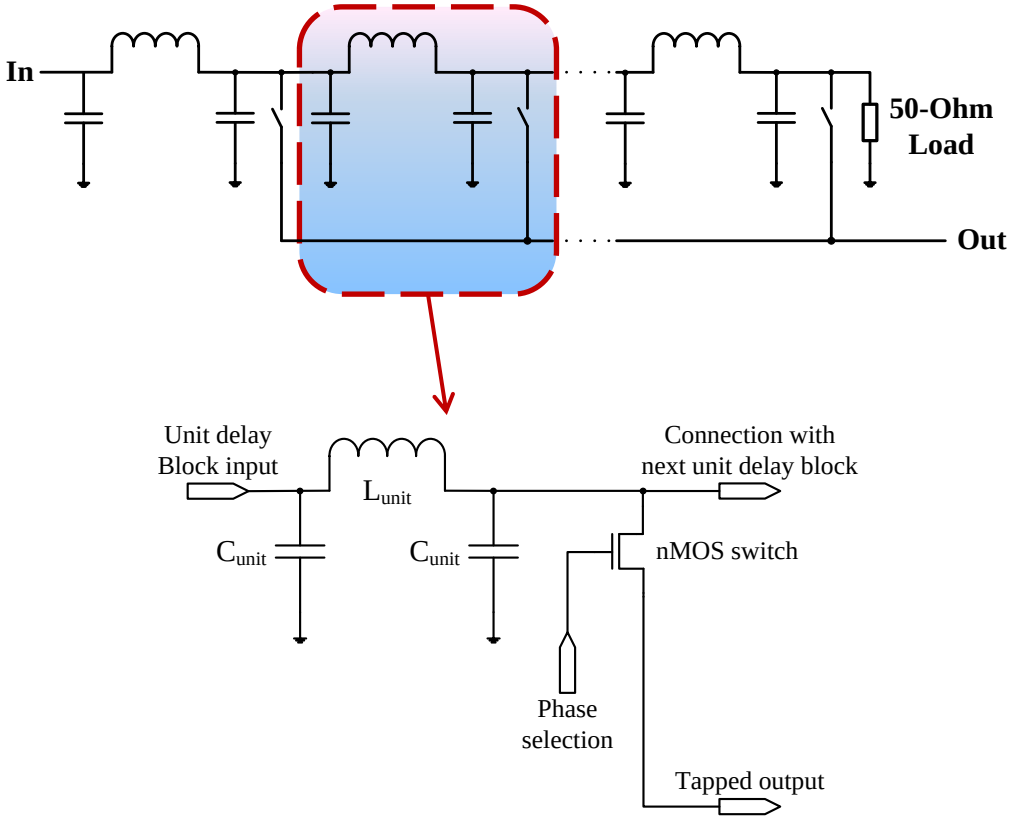
Ref. [16]:
All-Digital outphasing RF-PWM Modulator



- All-digital transmitters overview
- Digital to Time Conversion
  - All-Digital implementation
  - Mixed-Signal implementation
- Proposed mixed-signal Outphasing RF Pulse-Width Modulator
- Mixed-signal co-simulation environment and simulation results
- Conclusions

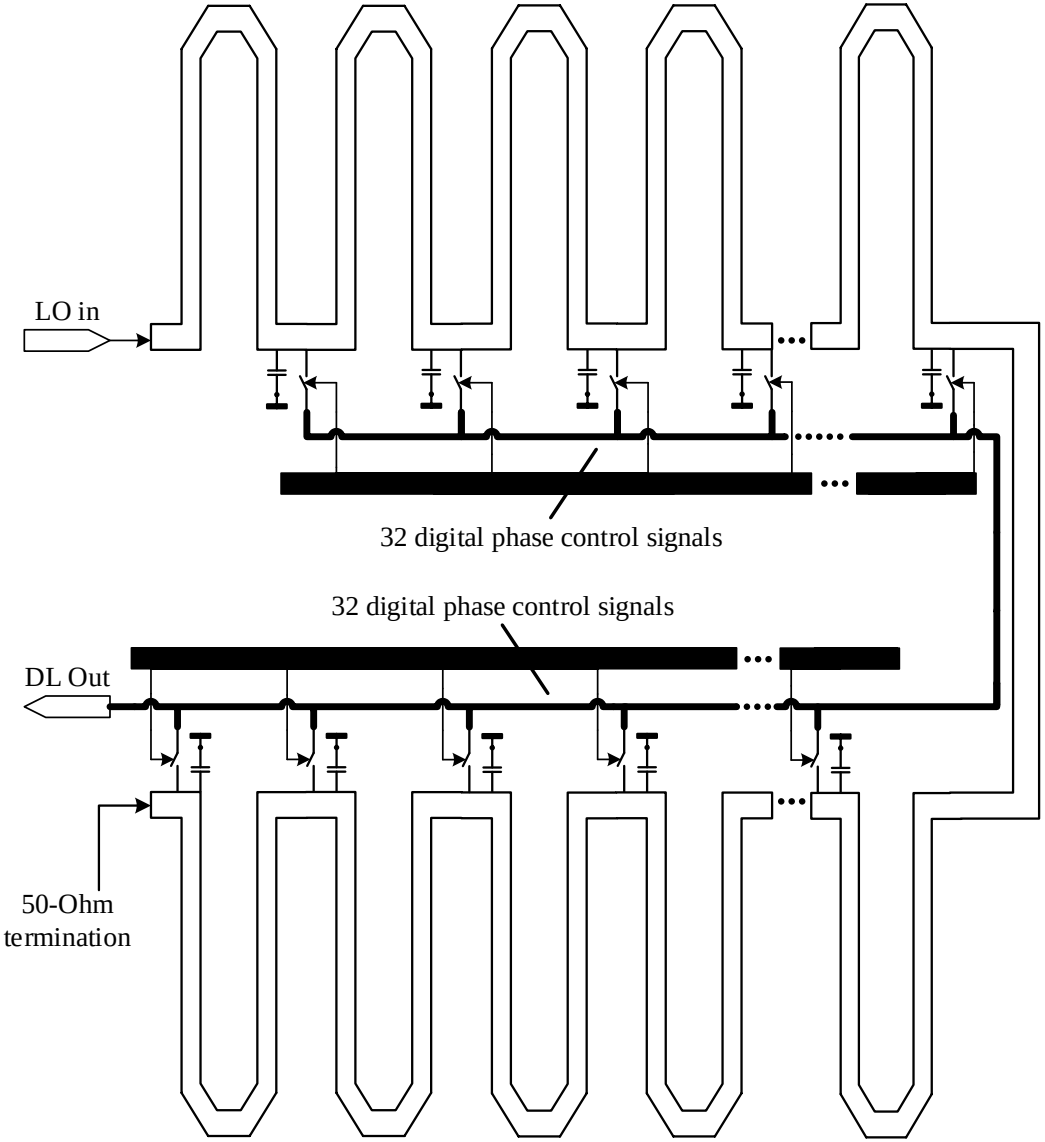
Continuous-Time Analog Phase Shifting

- LC Delay Line
- Distributed transmission line model
- RF carrier: Sine Wave



- "Hair Pin" integrated inductor
  - Minimal footprint
  - L_{unit} ~ 70 pH
- Time-delay step below 2 ps
  - Technology independent
  - PVT variation-resilient
- Small amplitude sinusoid
  - For mitigating nonlinearities of conducting switch
  - Very low power consumed only on the termination resistors

Floorplan of mixed-signal Phase-Shifting core

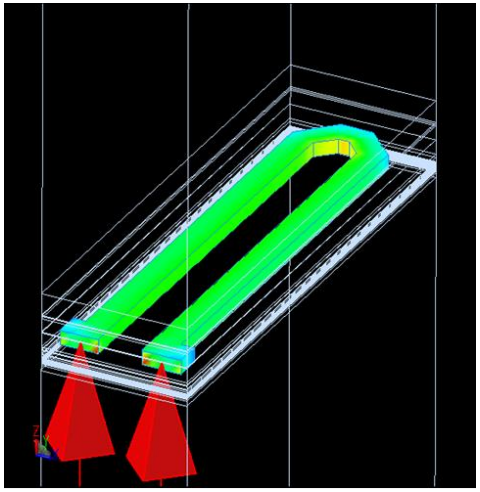


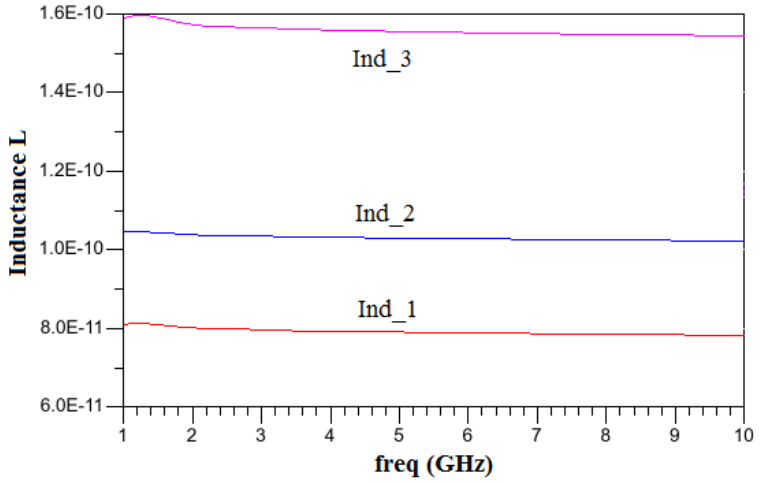
- One-hot switching scheme
- One-level multiplexing scheme

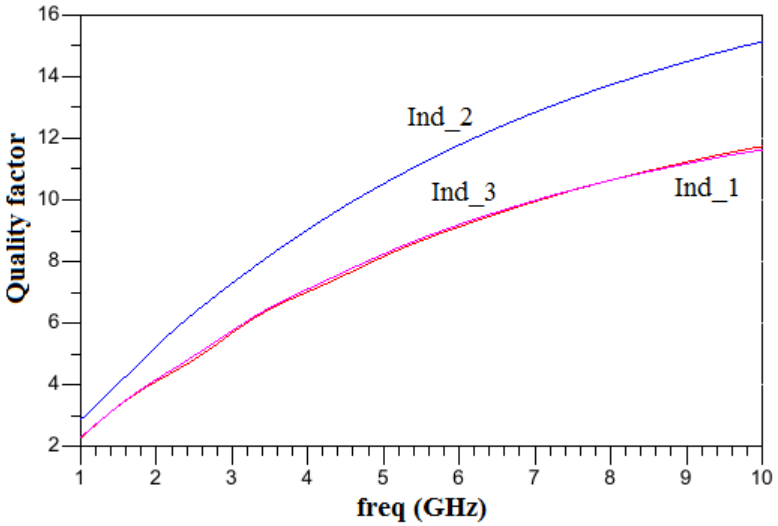
- 8-bit time resolution
- Carrier: 2.65 GHz
- Synchronous continuous-time operation (CLK - LO)

- Trade-off due to output common node parasitics
  - Frequency range
  - Time resolution
  - Dynamic behavior

“Hair Pin” integrated inductor





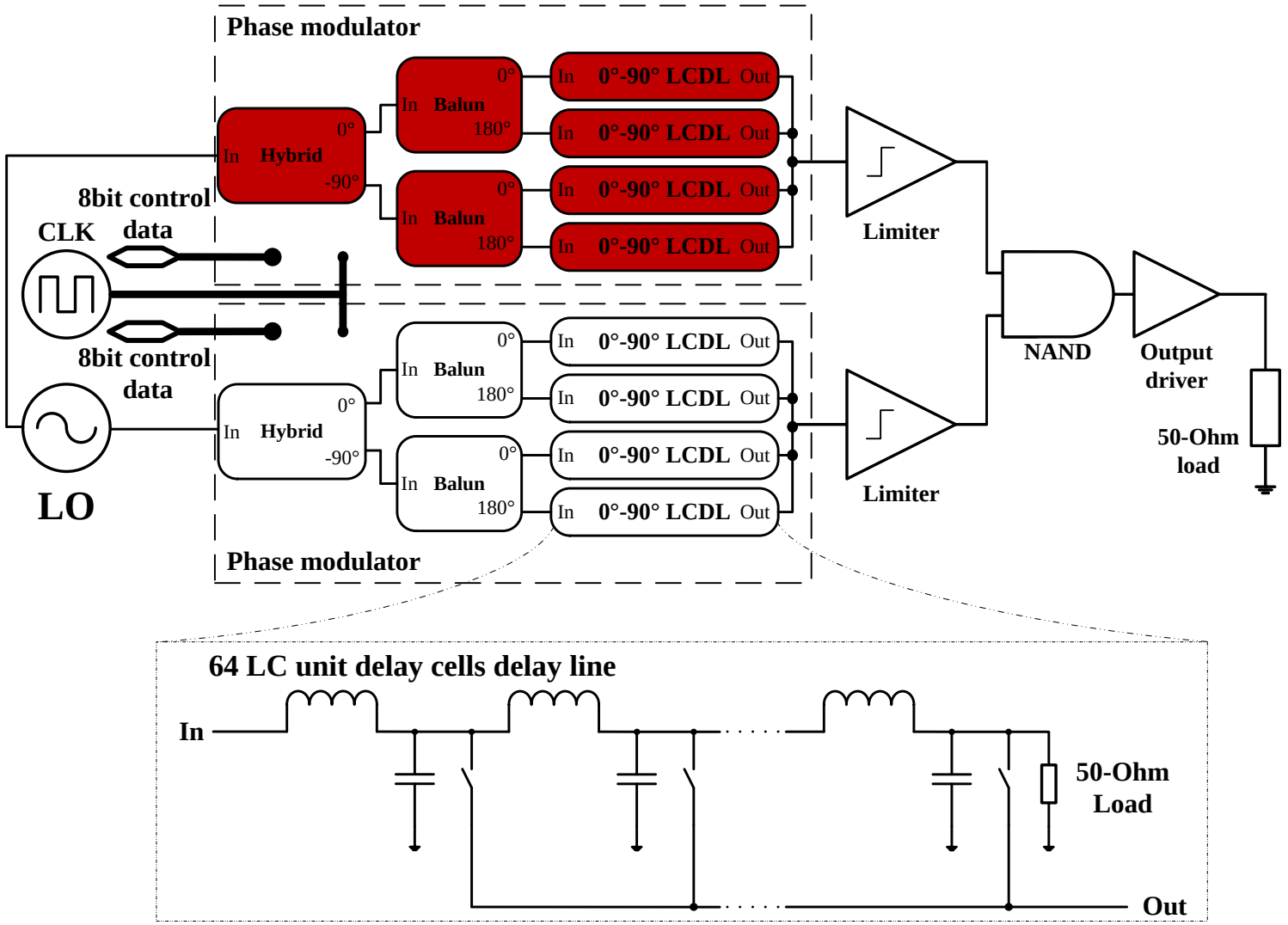


- $Ind\_1_{Xdimension} = Ind\_3_{Xdimension}$
- $Ind\_1_{Ydimension} = Ind\_2_{Ydimension}$

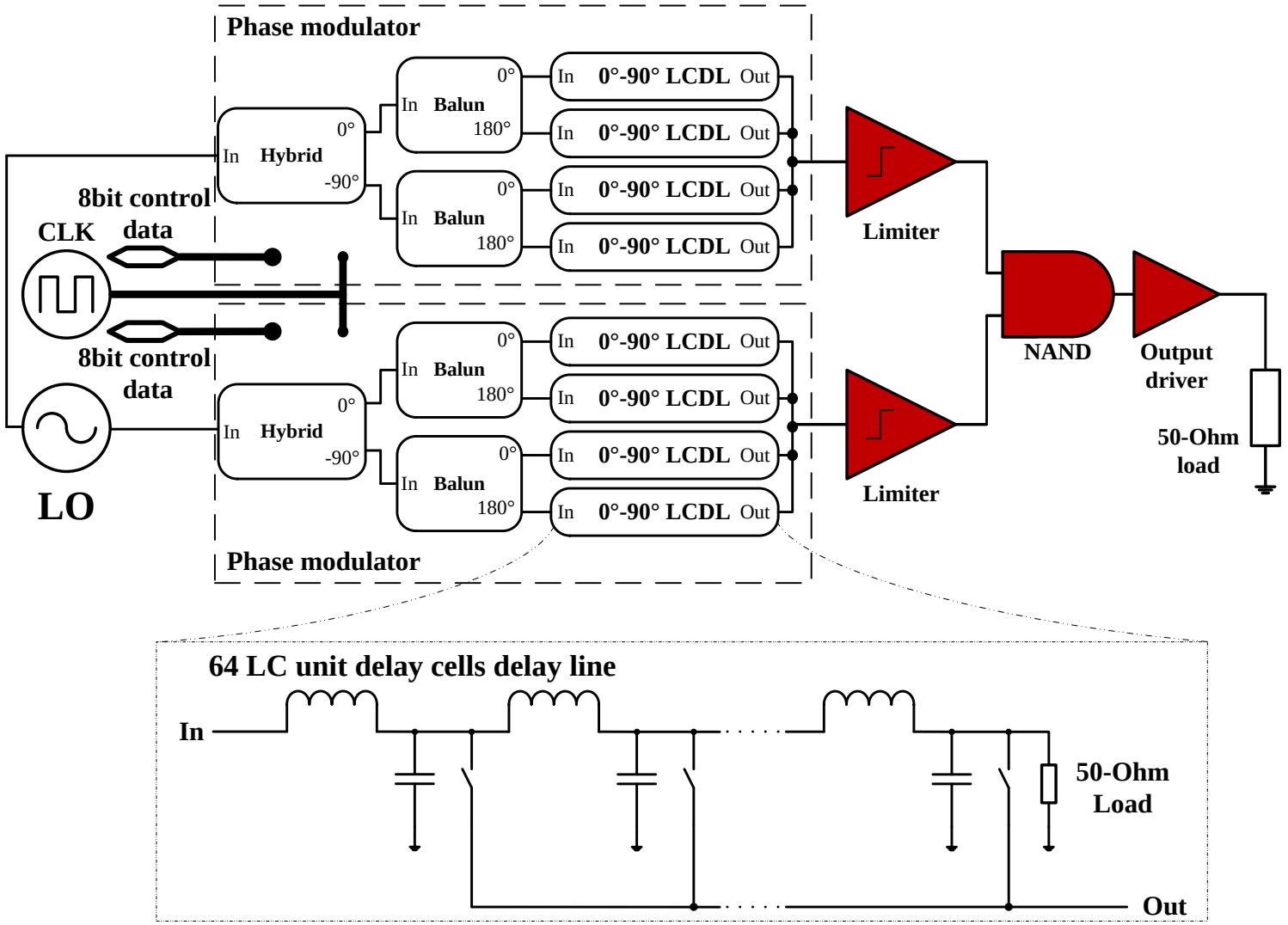
- Minimal X dimension
  1. Compact layout
  2. Interconnection parasitics minimization
     - Higher time resolution
     - Better dynamic response for the phase modulator

- All-digital transmitters overview
- Digital to Time Conversion
- Proposed mixed-signal Outphasing RF Pulse-Width Modulator
- Mixed-signal co-simulation environment and simulation results
- Conclusions

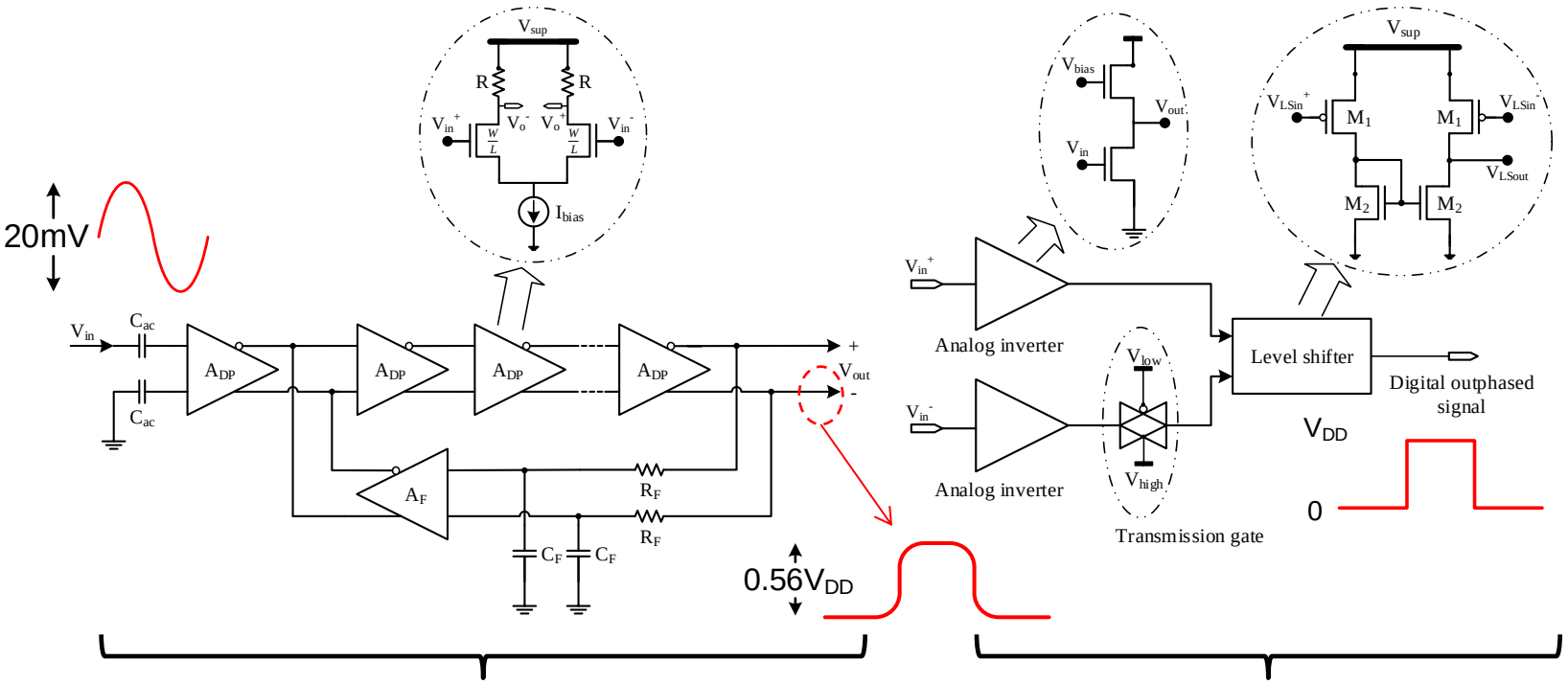
Mixed-signal Outphasing RF PWM Modulator



Mixed-signal Outphasing RF PWM Modulator



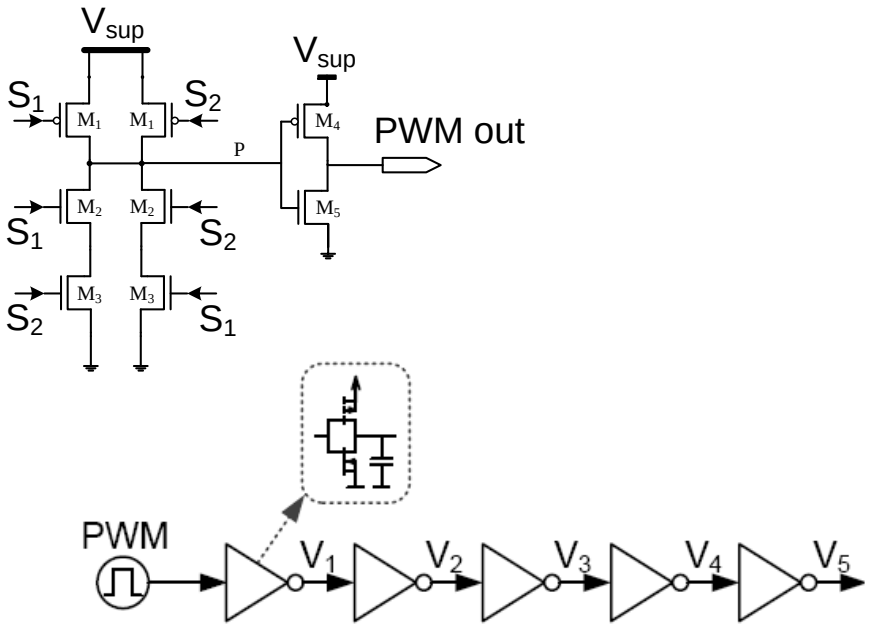
PWM signal generation: Limiter

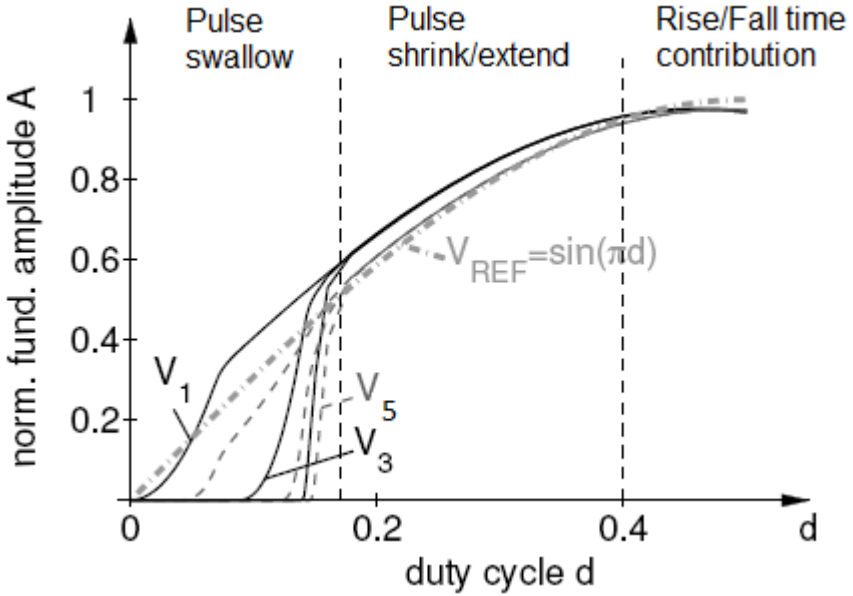


- Amplification to saturating levels of the input sine wave
- Maximum bandwidth design

- Generation of single ended continuous-time digital signal

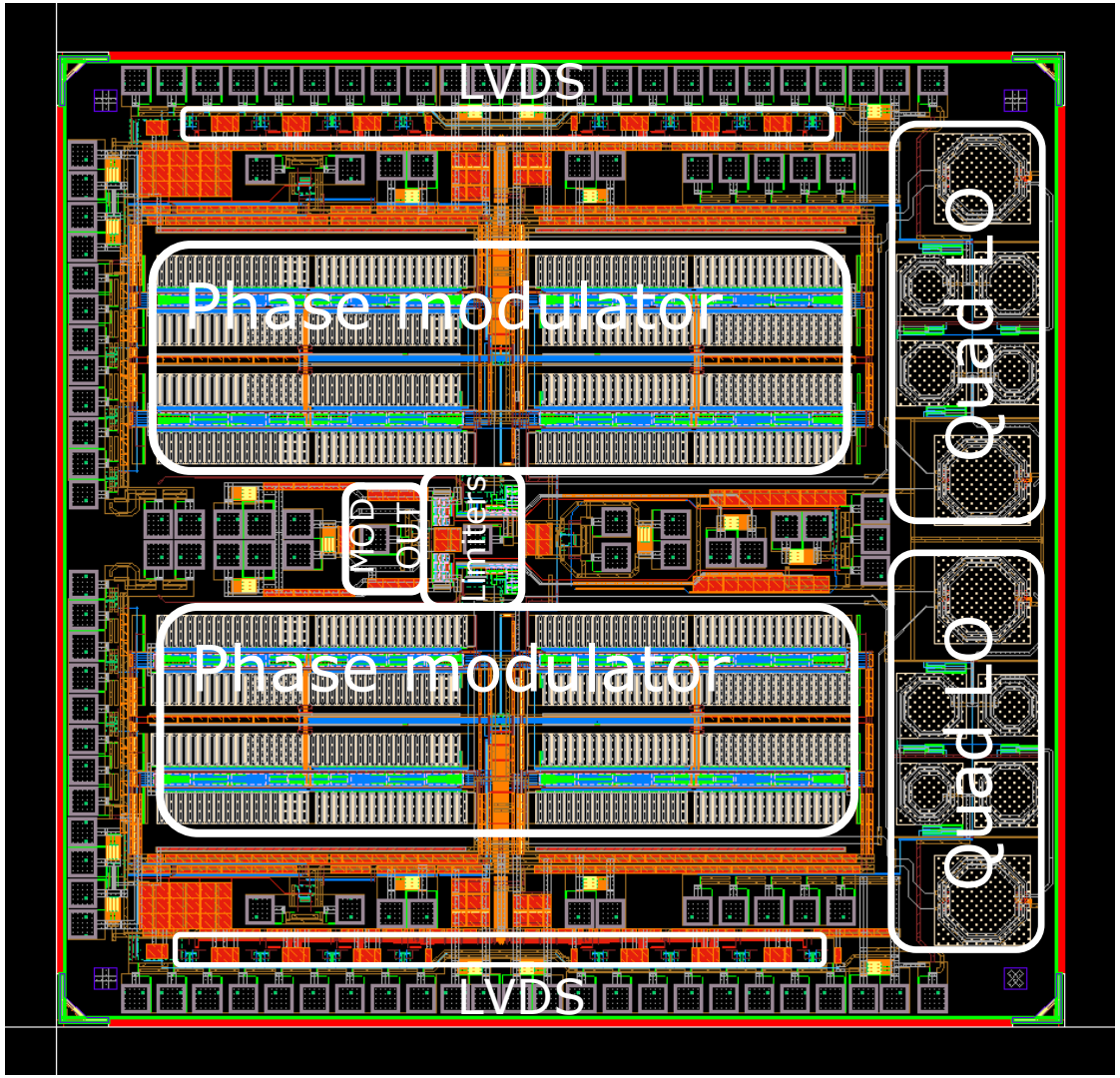
PWM signal generation: NAND gate / Output Driver Distortion





Pulse swallowing region	Pulse shrink/extend region
Minimum number of output driving elements	Equal rise/fall times @ NAND inputs
As small as possible rise/fall times @ NAND inputs	As small as possible rise/fall times @ NAND inputs

Mixed-signal Outphasing RF PWM Modulator



- Process: 40nm CMOS
- Voltage Supply: 1.25 V

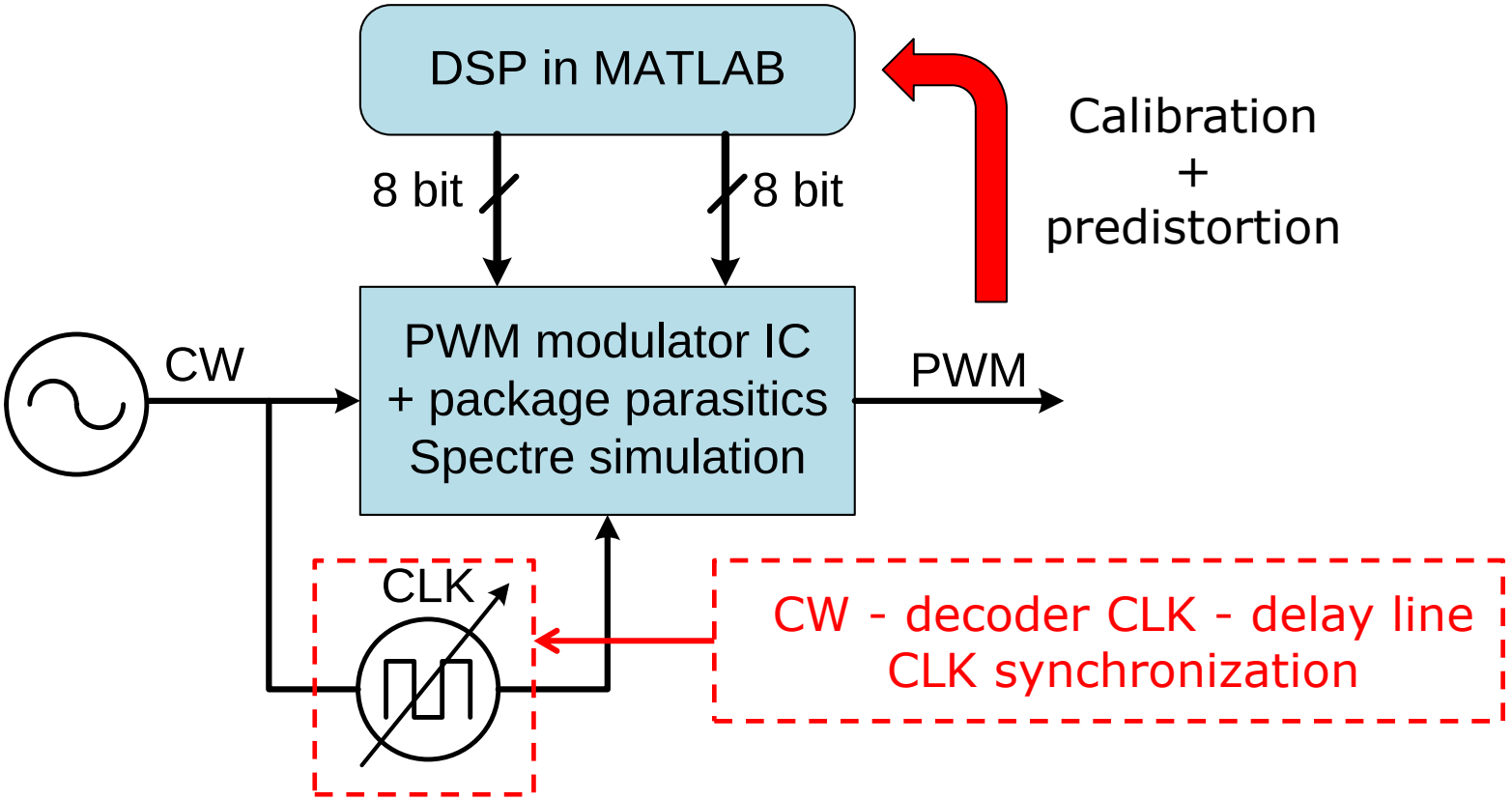
Modulator:
Power consumption

Part	Power consumption (mW)
Delay Lines	Nearly zero
Clock Distribution Tree, decoders, retiming circuitry *	107
Limiters	64
PWM generation	8
TOTAL	**179**
All Digital Outphasing RF PWM 40nm chip TOTAL power consumption for the same bandwidth and carrier frequency (Ref. [16])	**120**

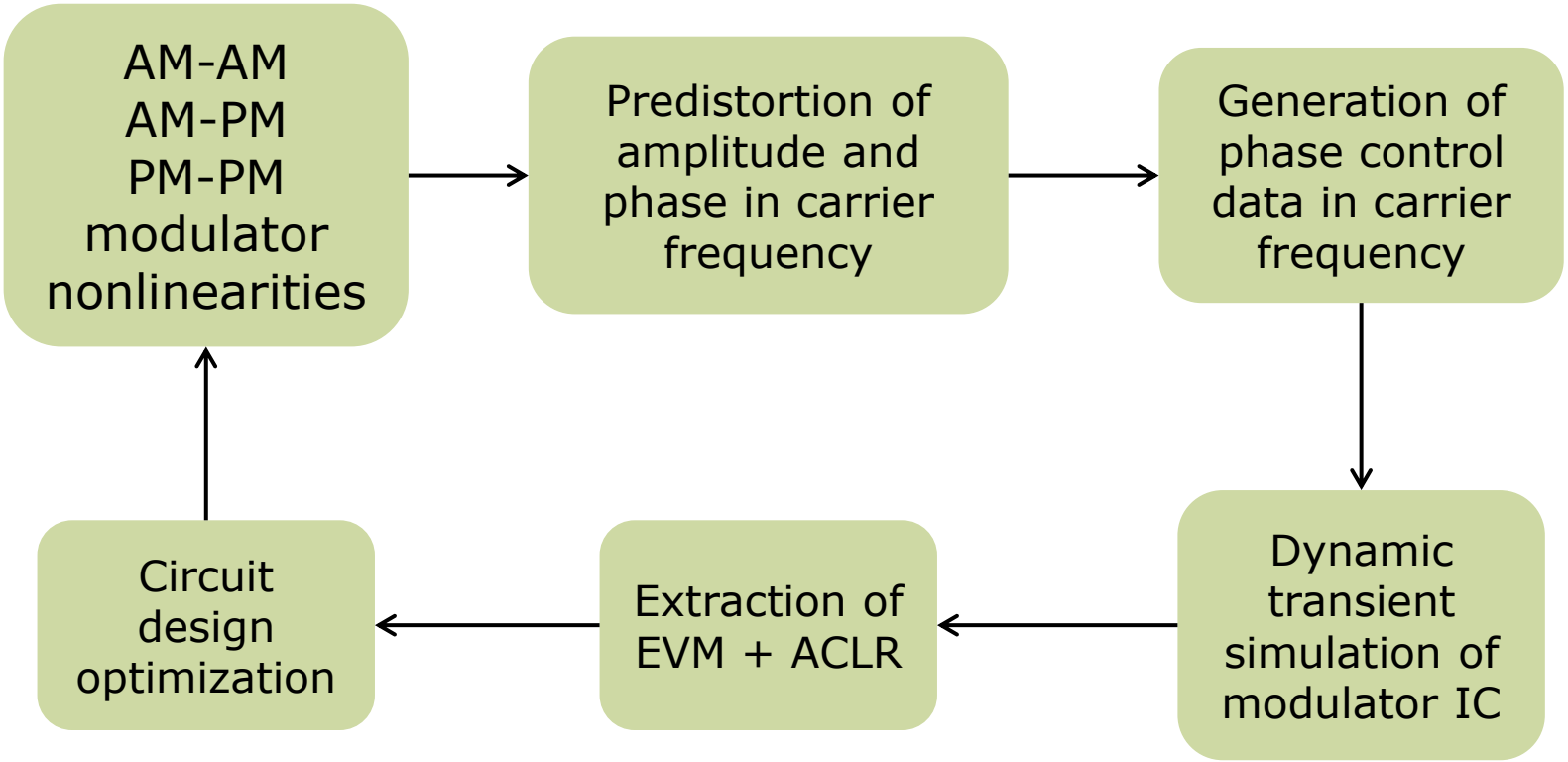
* Conservative design to assure predicted performance
(test chip for proof of concept)

- All-digital transmitters overview
- Digital to Time Conversion
- Proposed mixed-signal Outphasing RF Pulse-Width Modulator
- Mixed-signal co-simulation environment and simulation results
- Conclusions

Dynamic Performance Simulation

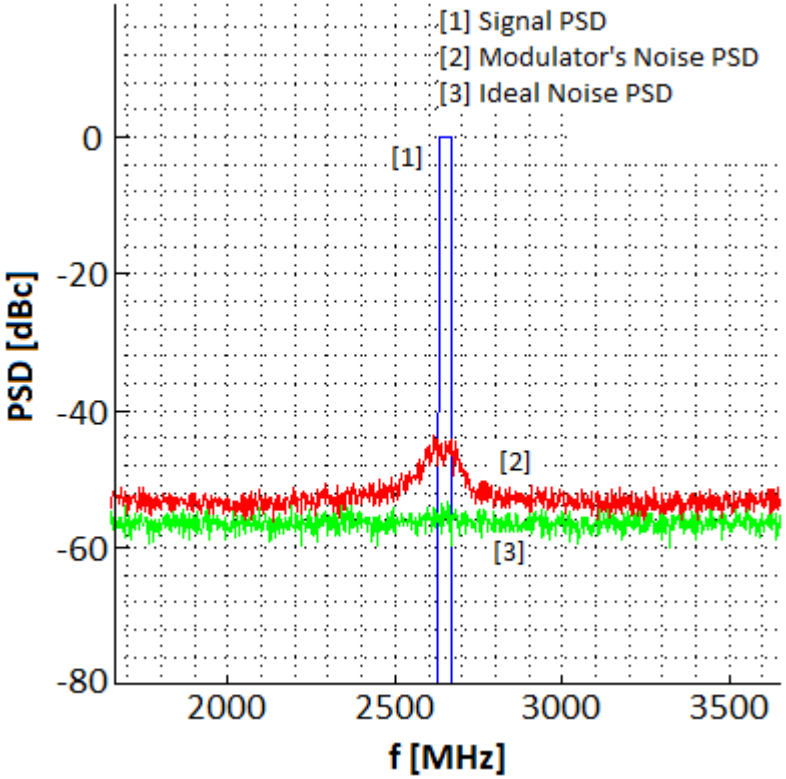


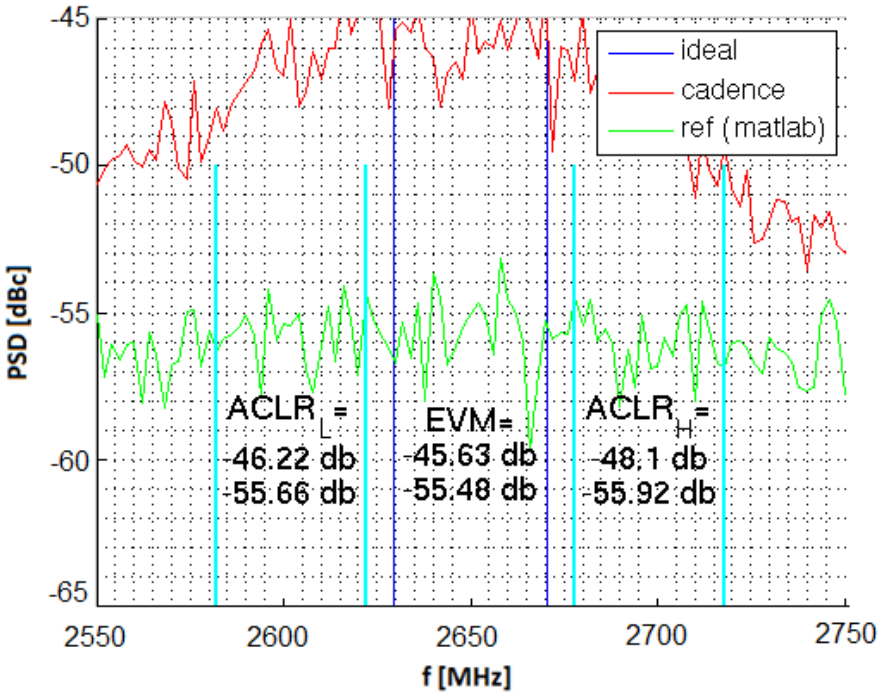
Dynamic Performance Simulation



Post-layout dynamic simulation results of modulator IC

- 20 MHz baseband signal (10 tones)
- 2.65 GHz carrier





Conclusions

- Mixed-Signal outphasing PWM modulator
- "Hair Pin" inductors
  - Minimal footprint
  - Silicon implementation of analog LC delay lines
- 8-bit time resolution
  - PVT variation-resilient
  - Technology independent
  - Low power consumption in the delay lines
- Simulated EVM = - 45 dBc
  - 20 MHz baseband signal on a 2.65 GHz carrier
- IC under fabrication
- Pending measurements

References

1. P. Eloranta *et. all*, "A multimode transmitter in 0.13 µm CMOS using direct-digital RF modulator", *IEEE J. Solid-State Circuits*, vol. 42, no. 12, Dec. 2007.
2. A. Jerng, and C. Sodini, "A wideband ΔΣ digital-RF modulator for high data rate transmitters," *IEEE J. Solid-State Circuits*, vol. 42, no. 8, Aug. 2007.
3. M. S. Alavi *et. all*, "A wideband 2×13-bit all-digital I/Q RF-DAC," IEEE Trans. on Microwave Theory and Techniques, vol. 62, no. 4, Apr. 2014, pp. 732-752.
4. V. K. Parikh *et. all*, "A fully digital architecture for wireless transmitters," in *Proc. IEEE Radio and Wireless Symp.*, Jan. 2008, pp. 147-150.
5. R. B. Staszewski *et. all*, "All-digital TX frequency synthesizer and discrete-time receiver for bluetooth in 130-nm CMOS," *IEEE. J. Solid-State Circuits*, vol. 39, no. 12, Dec. 2004.
6. P. Cruise *et. all,* "A digital-to-RF-amplitude converter for GSM/GPRS/EDGE in 90-nm digital CMOS," in *Proc. IEEE Radio Frequency Integr. Circuits Symp.*, Jun. 2005, pp. 21-24.
7. R. B. Staszewski *et. all*, "All-digital PLL and transmitter for mobile phones," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, Dec. 2005.
8. Z. Boos *et. all*," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, San Fransisco, CA, Feb. 2011, pp. 376-378.

References

9. J. Mehta *et. all*, "A 0.8mm^2 all-digital SAW-less polar transmitter in 65nm EDGE SoC," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, San Fransisco, CA, Feb. 2010, pp. 58-59.

10. M. Park *et.all*, "An amplitude resolution improvement of an RF-DAC employing pulsewidth modulation," *IEEE Trans. Circuits and Systems I: Reg. Papers*, vol. 58, no. 11, Jun. 2011, pp. 2590-2603.

11. Y.-C. Choi *et. all*, "A fully digital polar transmitter using a digital-to-time converter for high data rate system," in *Proc. IEEE Radio Frequency Integr. Technology Symp.*, Dec. 2009, pp. 56-59.

12. M. E. Heidari *et. all*, "All-digital outphasing modulator for a software-defined transmitter," *IEEE J. Solid-State Circuits*, vol. 44, no. 4, Apr. 2009.

13. A. Ravi *et. all*, "A 2.4-GHz 20-40-MHz channel WLAN digital outphasing transmitter utilizing a delay-based wideband phase modulator in 32-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, Dec. 2012.

14. P. A. J. Nuyts *et. all*, "A fully digital delay line based GHz range multimode transmitter front-end in 65-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 47, no. 7, Jul. 2012.

15. P. A. J. Nuyts *et. all*, "A fully digital PWM-based 1 to 3 GHz multistandard transmitter in 40-nm CMOS," in *Proc. IEEE Radio Frequency Integr. Circuits Symp.*, Jun. 2013, pp. 419-422.

16. S. Kulkarni, I. Kazi, D. Seebacher, P. Singerl, F. Dielacher, P. Reynaert, and W. Dehaene, "Multi-standard wideband OFDM RF-PWM transmitter in 40nm CMOS, in *Proc. IEEE ESSCIRC*, Sep. 2015, pp. 88-91.

Thank you

Part of your life. Part of tomorrow.

Infineon