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D2.7

Description of circuit design and test design of a novel power efficient and flexible transmitter system for MaMi based transmission

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Executive Summary

This report thoroughly describes the implementation level details of the chips fabricated in the context of MAMMOET project. Two different chips with the same output goal are described. The first chip is a fully digital implementation of a transmitter based on the RF-PWM and outphasing principle. All the elements on chip are digital and the final output signal is able to drive a switched mode Power Amplifier (PA). The second mixed signal chip is based on the same principle but the modulation is achieved using on chip passive components aiming to a low power implementation. In the first section a brief introduction is given about the outphasing principle. Although this has also been described previously in other deliverables, it is mentioned here again briefly just for the ease of the reader. The second chapter describes in detail the circuit implementation of the fully digital RF-PWM modulator along with the PCB (Printed Circuit Board) design. The third chapter is dedicated to the mixed signal RF PWM chip and the test setup developed for measuring it. The all digital modulator has been tested with WLAN signals and DMT signals and its performance is documented in the deliverable 4.3.

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Chapter 1 Introduction

Before going into the circuit level implementation details which is the objective of this deliverable, it is useful to revise the principle of operation of outphasing transmitters.

In traditional I/Q front-ends, the in-phase (I) and quadrature (Q) components are low bandwidth signals. When upconverted to the carrier frequency, the resulting signal is an amplitude and phase modulated signal, which is amplified at the next level. Because of the amplitude modulation, the power amplifier (PA) efficiency is significantly reduced as it has to operate at a certain back-off due to the high peak to average power ratio (PAPR) of signals like WLAN OFDM.

An alternative to this approach is the outphasing based transmitter which uses constant envelope, phase modulated signals.

Two constant magnitude vectors (s1, s2) can be rotated to generate a point in the IQ plane as shown in Figure 1.

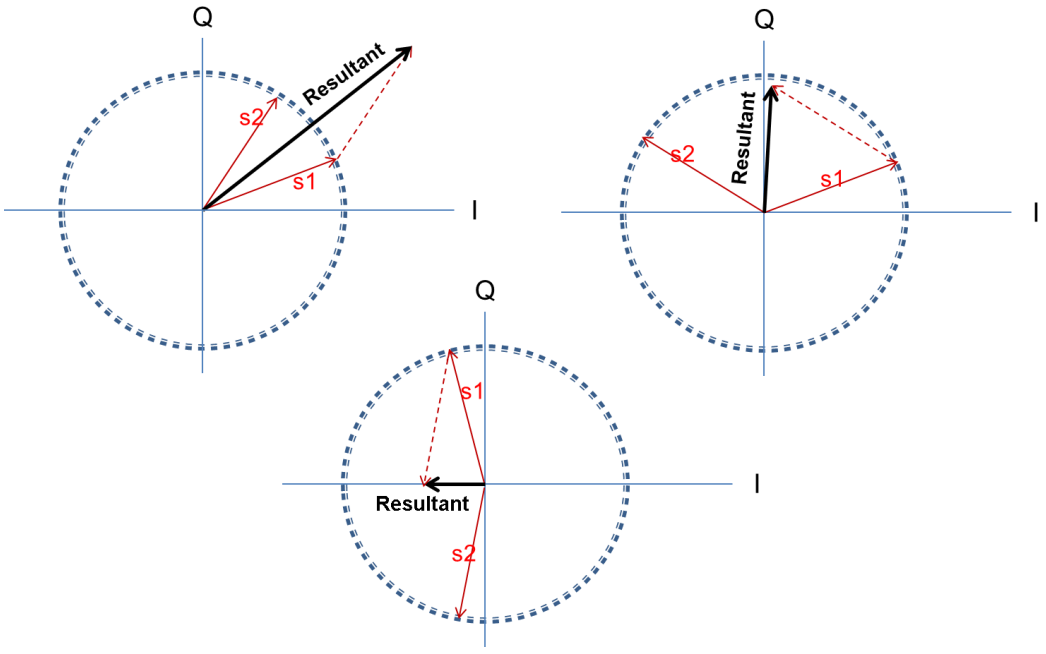

Figure 1 Generation of a point in the IQ plane using constant envelope signals.

The downside of using outphasing signals is that there is considerable bandwidth expansion when I/Q signals are converted to outphasing signal. This is because of the non linear conversion of I/Q components to amplitude and phase signals. The bandwidth expansion of the amplitude and phase signals as compared to the in-phase signal is shown in Figure 2.

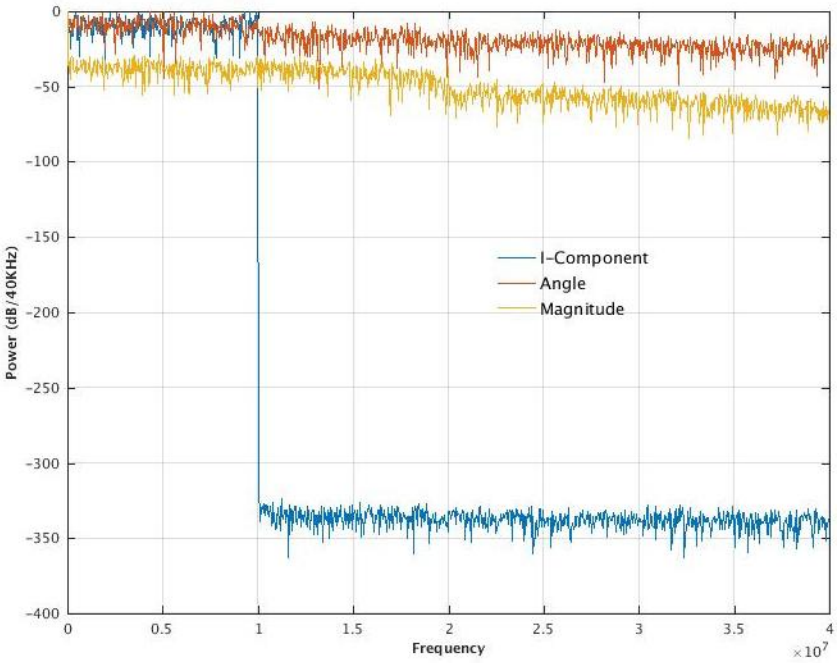

Figure 2 Bandwidth expansion of angle and mag

So outphasing transmitters combine two non-linear signals to make one linear signal and any mismatch or errors in the recombination increase the noise floor and cause leakage in to the adjacent channel.

In MAMMOET a total of two different tape outs were done. One of the chips is a mixed signal design and the other one is a full digital transmitter. In Chapter 2, the detail implementation of the full digital modulator is given and in Chapter 3 the mixed signal design is discussed, followed by a conclusion. The measurement results of the digital transmitter are documented in D4.3 “Proof of concept of innovative hardware including transmitter characterisation”.

Chapter 2 Digital RF-PWM Transmitter

In this chapter the digital RF-PWM tapeout done under the MAMMOET project is described at the implementation level.

As has been discussed in previous deliverables, D2.5 “Description of MaMi digital modulation and architectures for efficient MaMi transmission” and review meetings, the type of circuits used come under the category of “time based signal processing digital circuits”. This concept enables the information to be stored in the position of the edges of a digital signal. To encode the carrier information (phase and amplitude) in a digital signal, the position of the rising and falling edges within a carrier period correspond to the final amplitude and phase of a sinusoidal carrier. This is best explained by looking at the Fourier expansion of a pulse width modulated (PWM) square wave which is given as:

$$f(t) = d(t) + \sum_{n=1}^{\infty} \left(\frac{2\pi}{n} (-1)^n \sin(n\pi d(t)) \cos(n\,\omega_o\, t \;\; + \varphi(t) \;) \right)$$

where d(t) is the time varying duty cycle. If this square wave is filtered after the PA only the fundamental (n = 1) component remains. This is a sinusoidal signal given by

$$\sin\left(\pi . d(t)\right) . \cos\left(\omega_o t + \varphi(t)\right)$$

where the time independent amplitude scaling term has been ignored. This is basically a sinusoidal carrier at frequency ω_o. This carrier signal has amplitude modulation which depends on the duty cycle of the square wave (d(t)), and phase modulation φ(t) which depends on the position of the pulse within a carrier period. Hence, by varying the duty cycle of a square wave which has the fundamental frequency of the desired carrier and the phase/position of the pulse within a period of the square wave we can get a sinusoidal signal with amplitude and phase modulation.

So at the heart of this circuit is a digital to time converter which here is implemented by means of a phase modulator. In Figure 3 a general overall picture of the system is given and a detailed description of the blocks follows.

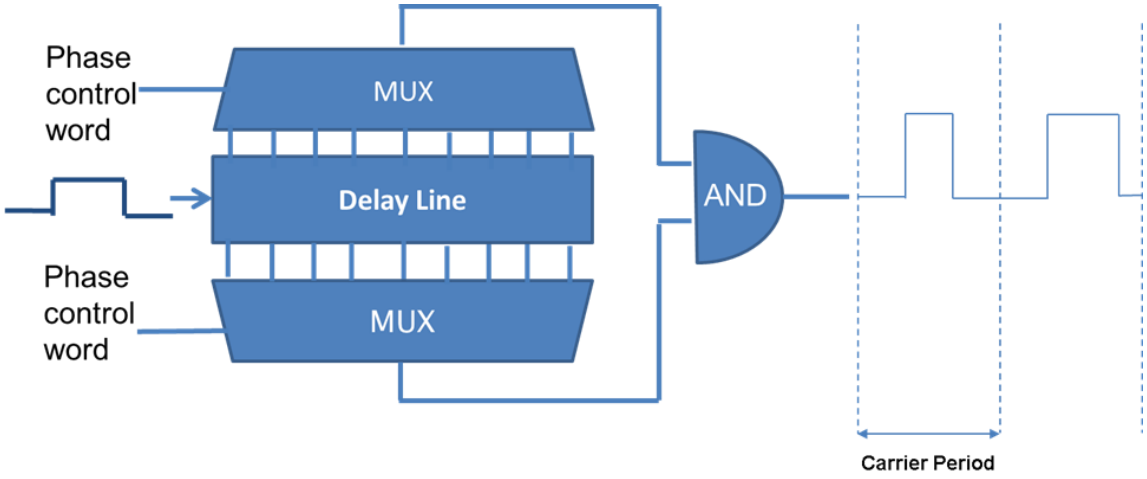

Figure 3 Generation of pulse width and phase modulated signals by using digital phase modulators

2.1 Circuit Building Blocks Description

In this section a description of the circuits is provided, starting from the phase modulator and moving towards the final output. The description of the circuits follows the path that the signal follows in the circuit.

2.1.1 Phase Modulator

As described above, the phase modulators and the multiplexers that are used to select the desired phase are at the heart of this system. A cross-coupled delay line based phase modulator is used as shown in Figure 4. One side of the delay line is used to generate the signal for the first outphasing path S1 and the other side is used to generate the signal for the second outphasing path S2. The small cross coupling inverters in between ensure that the phase mismatch between the S1 and S2 paths is minimized. The length of the delay line in this design is 32 elements. Each delay element provides a delay of 16 ps. This means that using the delay line with 32 delay units the maximum delay is 16ps x 32 = 512ps. Considering a carrier signal of frequency 1/512e-12 = 1.9531 GHz, we can get a full 360 phase coverage from only the delay line at this frequency. The resolution will be (2^5 = 32) 5 bits. At higher frequencies this resolution will further decrease.

From the standalone delay line the minimum carrier frequency that can be used is 1.9531GHz at 5 bits of resolution. Circuit level techniques that extend the range of the delay line without adding extra stages and also a way to increase the resolution will be described later on.

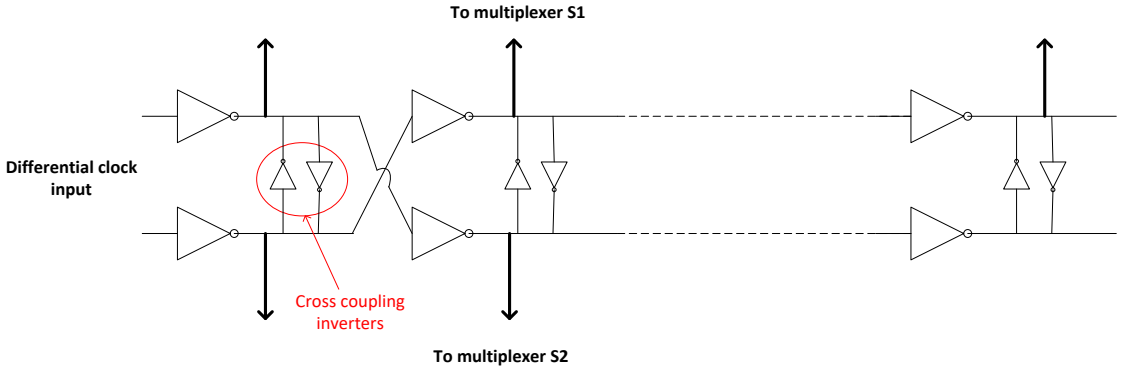

Figure 4 Cross coupled delay line

2.1.2 Multiplexers

Regarding the design of the multiplexers, for selecting the appropriate phase based on the control word, great care was taken during layout to match the path length and path delays from of each of the 32 possible paths that the signal can take, in order to minimize mismatch based errors. The basic unit of the multiplexer is a transmission gate based buffer and switch, as shown in Figure 5.

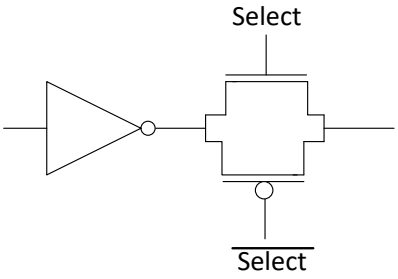

Figure 5 Basic switch based on transmission gate

Connecting two of them together results to a 2:1 multiplexer (Mux) and connecting 4 together results to a 4:1 Mux. As an example a 4:1 Mux is shown in Figure 6.

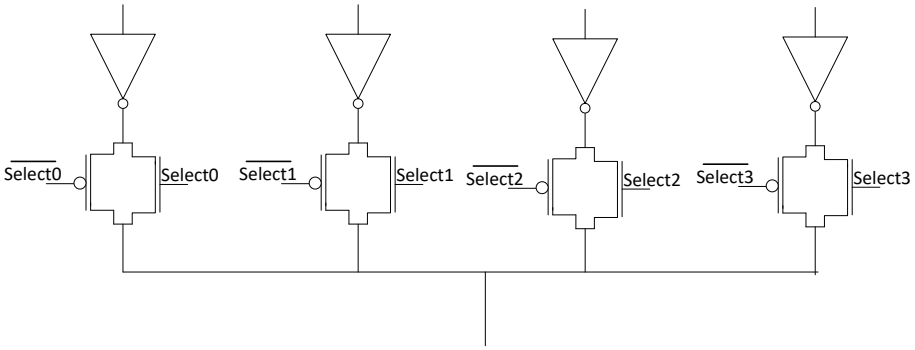

Figure 6 A 4:1 Mux based on transmission gates

Using a transmission gate based switch instead of just using a single NMOS or a single PMOS based switch, gives better performance as the full VDD and zero level can be used. Monte Carlo simulations for mismatch variations show that this gives better performance in terms of matching, as the effective area of the switch has been doubled.

The multiplexer needed for this design is a 32:1 Mux, which can be built by connecting 8 of the 4:1 Muxes in parallel. However, simulations showed that if the 32:1 mux is implemented in just one layer, the capacitance at the output of the mux is so large that it is not possible to use it for high speed digital signals. In order to reduce this capacitive load, the multiplexer is broken down into three layers using 4:1 Muxes and a 2:1 mux as shown in Figure 8. After passing through the transmission gate, the rise and fall time of the signal increases. To restore fast edges, intermediate buffers are used, as shown in the Figure 8.

After these considerations, the block diagram at this point looks like as the one shown in Figure 7, where S1 and S2 are the two outphasing signals.

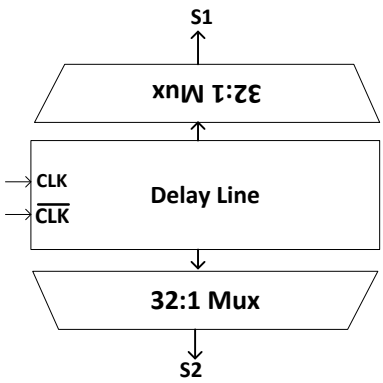

Figure 7 Delay line and multiplexer

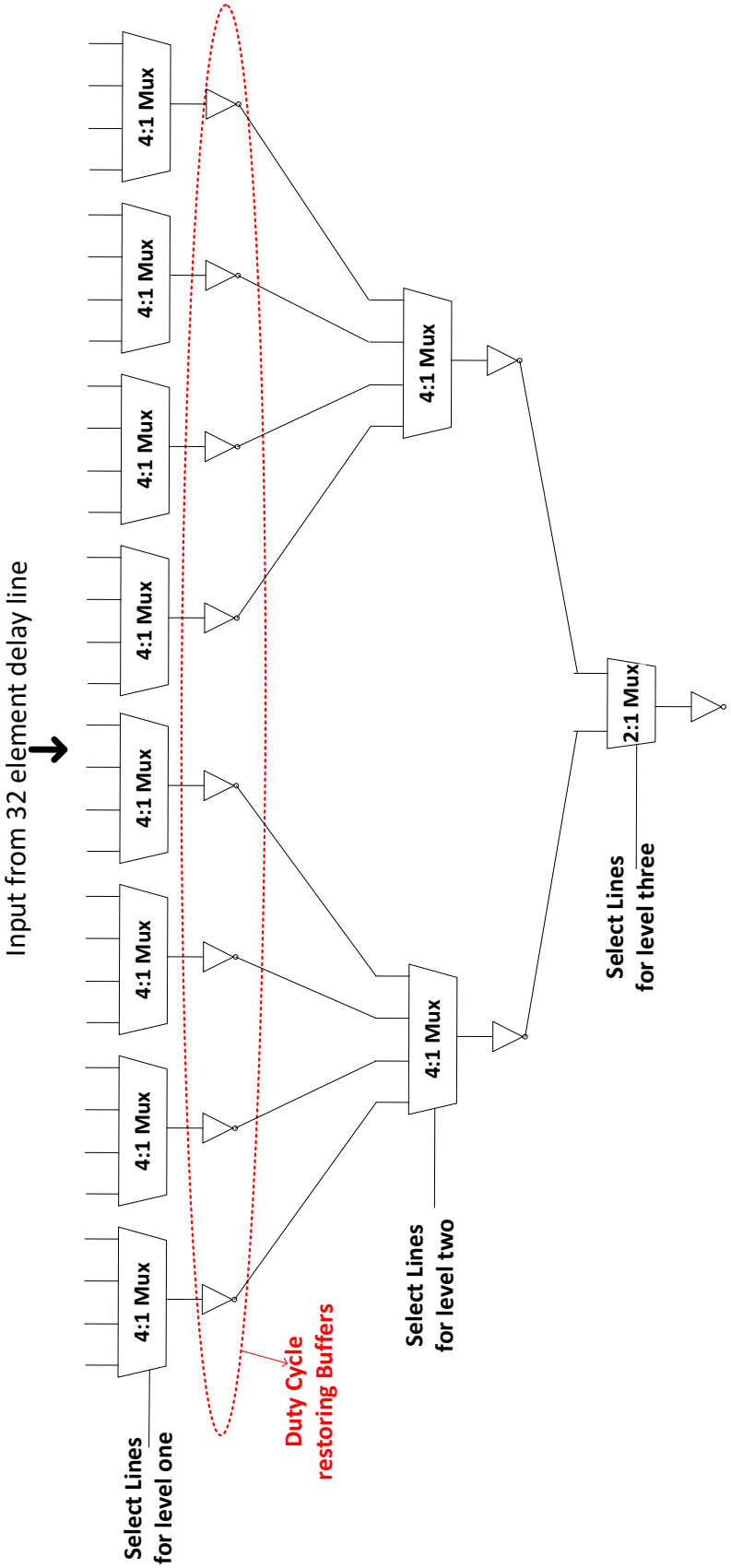

Figure 8 Multiplexer implemented as a tree mux

2.1.3 Increasing the Resolution

Using only CMOS inverters provides a resolution of 16ps, but this is not enough for the desired system performance at 2.4GHz carrier frequency. To increase the resolution, NMOS based varactors have been used after the 32:1 mux. The circuit configuration is shown in Figure 9.

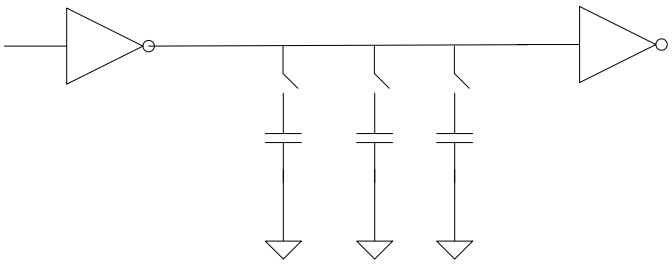

Figure 9 Changing capacitive load at the output of a buffer

The basic principle is that by changing the capacitive load at the output of a buffer we can increase and decrease the speed of the signal through it. The variable capacitors or varactors have been implemented using NMOS transistors. As shown in Figure 10 by changing the voltage at node B from VDD to 0 or vice versa, the gate to body capacitance is changed.

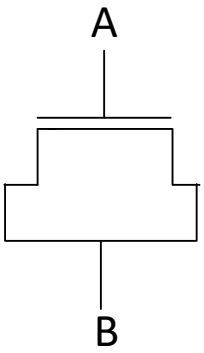

Figure 10 NMOS based varactor

Through this technique a resolution of 1 ps is achieved. Using varactors along with the delay line, a coarse-fine architecture has been implemented in which the delay line gives a 16ps resolution and the varactor stage gives a 1ps resolution. Now the number of varactors that are to be used has to cover the full 16ps delay of a single delay unit in the delay line. This means that 4 bits are necessary for the fine delay part, which translates to 4 binary weighted varactors. The problem with the binary weighted varactors is the large size and that, while jumping from one codeword to another codeword, there is considerable charge feed through into the signal path which disturbs the signal. Therefore instead of binary configuration, a thermometer coded configuration is used, where all of the varactors are of equal size. The charge feed through for the majority of code words is reduced thus giving a better signal integrity.

2.1.4 Extending Delay Line Range

As was discussed in the previous section, the lowest frequency of operation (dependent on the length of the delay line) is 1.9531 GHz. In order to lower this limit, the length of the delay line can be increased, which would also call for a larger Mux, thus increasing power consumption. This will also add more delay variability in the system because of the increased

number of signal paths. An alternative solution is to invert the signal and use just a single 2:1 mux to select between the inverted and non inverted signal.

This is made clear in Figure 11.

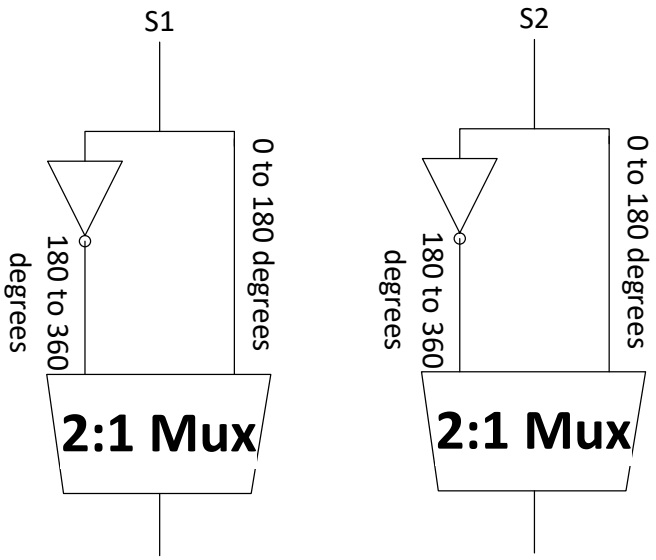

Figure 11 Lower frequency bound extension of delay line

Therefore, instead of getting the full 360 degrees from the delay line, it only needs to cover half the period (180 degrees) and the other half of the range can be provided from the circuit shown in Figure 11. This means that the lowest frequency that can be used now is 1.9531GHz/2 = 976.6 MHz.

The system level configuration with the frequency range extension and fine phase shift varactors is shown in Figure 12.

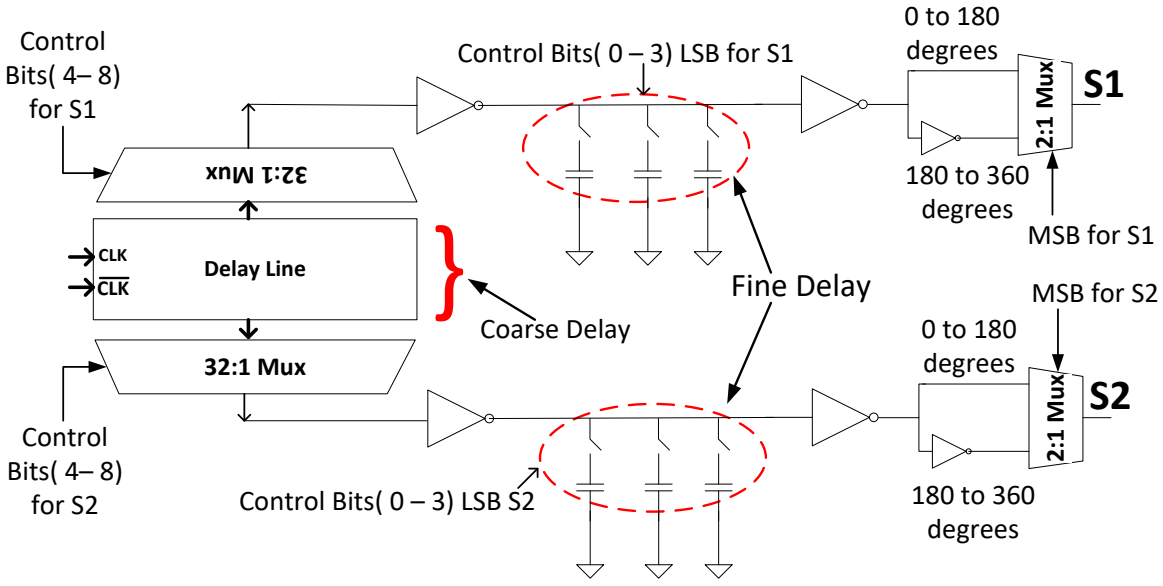

Figure 12 System level view with fine phase-shift varactors

2.1.5 Output Stage

The outputs (S1 and S2) from Figure 12 are applied to a symmetric NAND gate. A symmetric NAND gate is used in order to mitigate any data dependent effects on the signal. At the output of the NAND gate there are buffers to drive a 50 ohm load. As was discussed in previous deliverable (D2.5) and review meetings, along with the NAND gate output, the inputs to the NAND gate are also brought off-chip through 50 ohm drivers to implement off-chip outphasing in case of higher frequencies where RFPWM shows considerable pulse swallowing.

2.1.6 Control Data Timing

In the previous sections the signal path was described. It is a completely asynchronous digital design. In this section the path followed by control signals and their timing is presented. This path is partly synchronous and partly asynchronous.

The control signal path is shown in Figure 13. It starts by bringing the control signals from the PCB on the chip through aluminium bond wires. On the chip each differential data bit is picked up by a low voltage differential signalling (LVDS) receiver. The output of this receiver is regenerated using inverters to full scale and the data bits are clocked by the first stage of flip flops. The first stage of flip flop adds robustness against any mismatch in timing between the data bits that may be present due to external off chip systems. The area of the chip is determined by the number of bond pads. Although the core area of the chip is very small, the total area increases due to the bond pads. This means that data bits have to travel over a long distance to reach the modulator core from the bond pads. For high speed signals this distance can correspond to more than a clock cycle. This is why another layer of flip flops is added for robust timing between the first layer of flip flops at the IO's and the layer of flip flops at the input of the modulator. In a full system on chip implementation, these extra flip flops will not be needed.

Also the asynchronous part of the control signal paths has been minimized by placing the third and final layer of the flip-flops as close as possible to the modulator core, as shown in Figure 13.

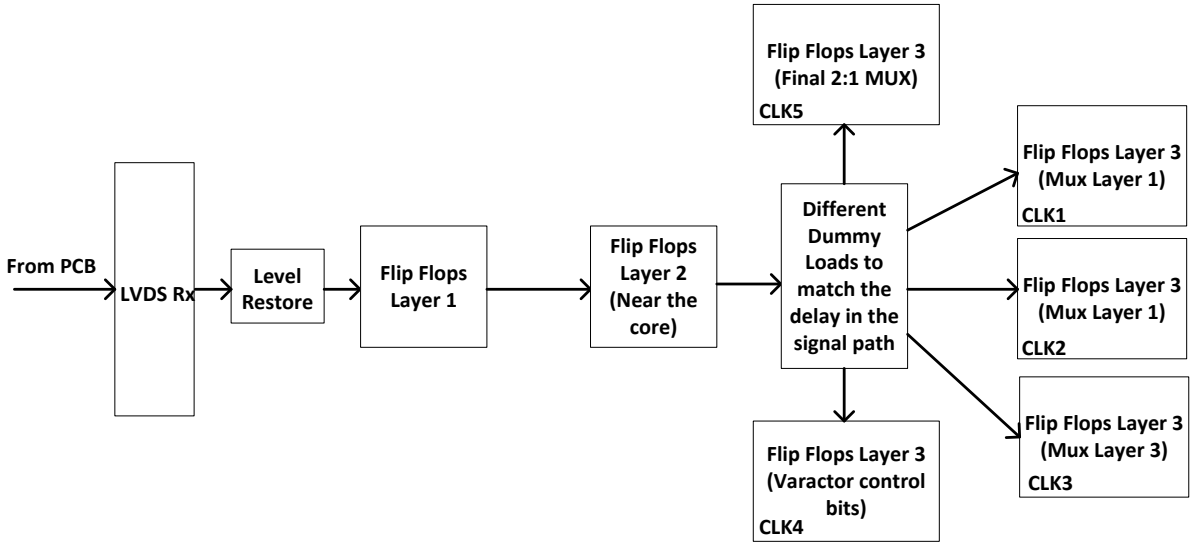

Figure 13 Control Data Path

In the third layer of flip flops, those flip-flops that correspond to each core element are clocked by clocks having different delays. The clocks and data signals are delayed by adding dummy elements in their path. The time by which each clock has to be delayed is determined

by the delay in the signal path. Namely the time that the signal (carrier) takes to travel from the output of the delay line to that point in the chip. This is why the data coming into the third layer of flip flops has to be delayed along with the flip flops by a safe margin.

2.2 Test System Design

In this section, the system and setup used in the testing of the all digital transmitter is described. A detailed description of the test setup is provided in D4.3. But just for the sake of continuity of D2.7 it has to be mentioned here that the data to be applied to the test chip is stored in a parallel data generator which has 16 output differential channels. Although the chip designed has 10 bits time resolution for each of the outphasing paths, the LSB currently can not be used due to limitation of the test equipment and, as a result, the resolution is limited to 2ps instead of the designed resolution of 1ps. The LSB resolution has been independently verified and will be used in the test setup in future testing.

2.2.1 PCB Design

Two PCB's are designed for the purpose of testing. One large PCB has 20 differential SMA jacks which receive the data from the parallel data generator. The large PCB is shown in Figure 14.

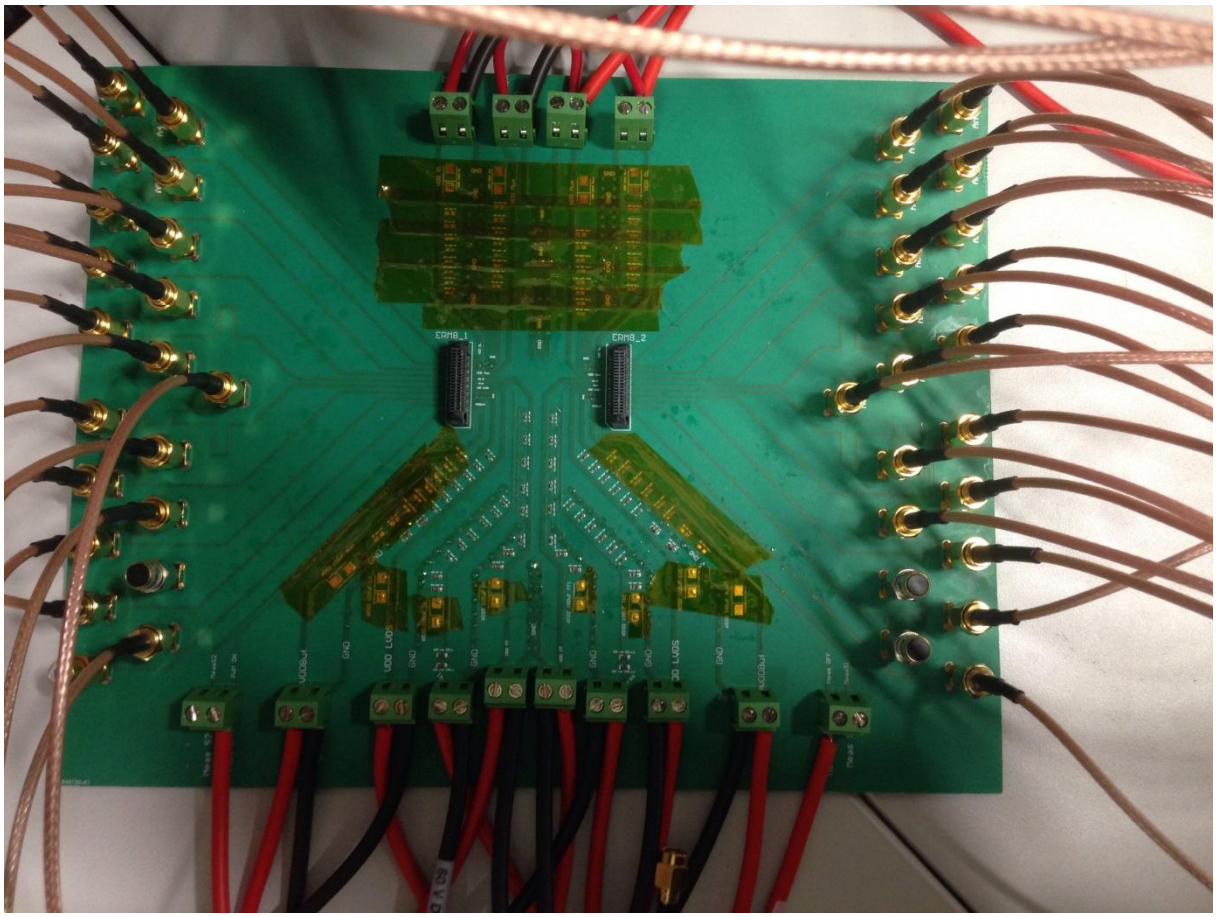

Figure 14 Main PCB

This large main PCB also has supply decoupling capacitors for the synchronous circuits, connectors to the power supplies and two high speed PCB to PCB connectors through which data bits travel from the main to the secondary PCB which sits on top of it having the modulator chip mounted on it.

The small secondary PCB is show in Figure 15. It has the chip mounted on it. On the bottom side of this PCB there are decoupling capacitors for the sensitive asynchronous part of the circuit. It also has high speed SMA connector for the differential clock input and three SMA connectors for the RF-PWM S1 and S2 output signals. Also care has been taken to match the path lengths of the data signals on the PCB as much as possible.

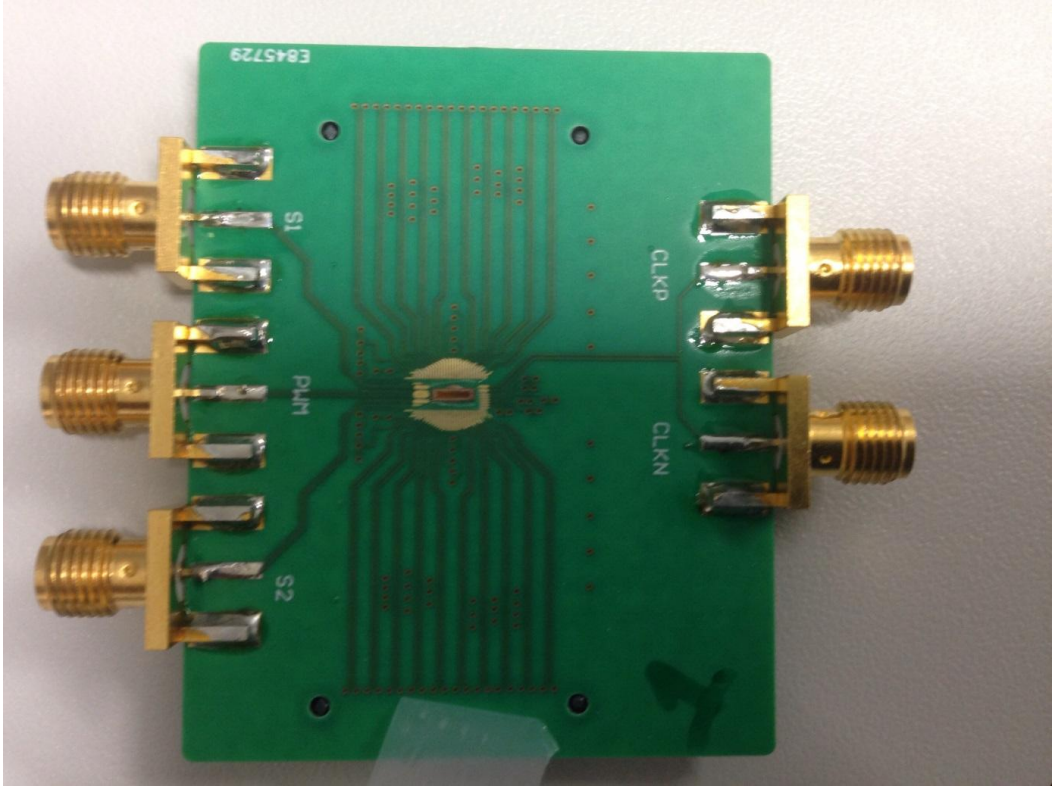

Figure 15 Secondary PCB

In Figure 16 the chip with bond wires is shown. The picture was taken using a digital microscope.

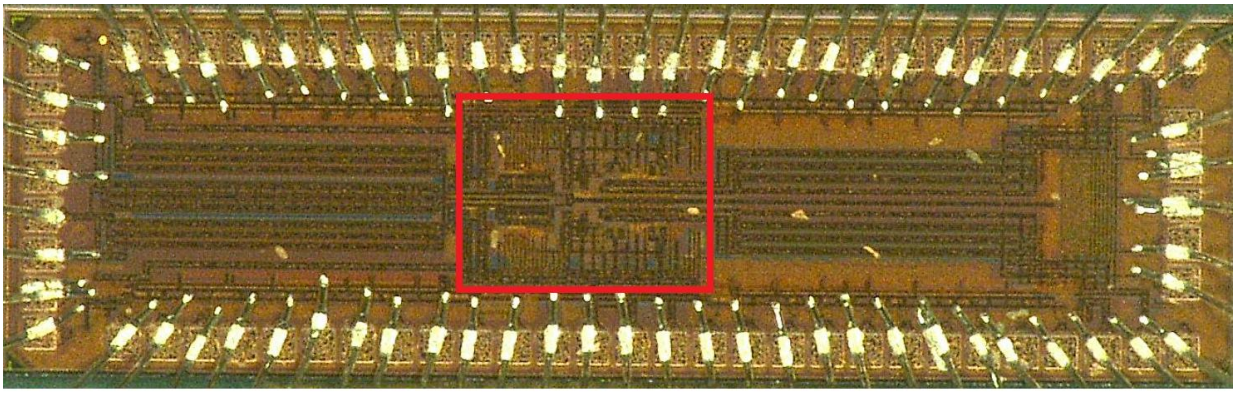

Figure 16 Chip wire bonded onto the PCB

2.2.2 Test Cycle

The test flow is shown in the figure below:

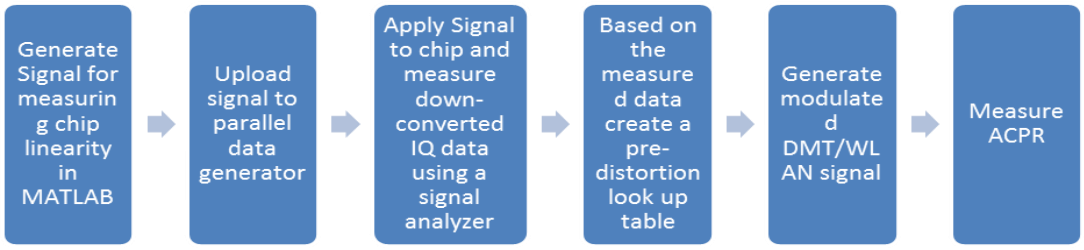

Figure 17 Test flow

At first, a signal having a bandwidth of 10MHz is generated in MATLAB from which the control signals to the outphasing vectors are created. These control signals are then applied to the test chip at the desired carrier frequency. The output of the chip is the carrier signal modulated with the test data. This output is measured using a signal analyzer which downconverts the carrier signal and extracts the IQ data. The IQ data is sent back to MATLAB where a look up table is generated based on this data. Then control signals for modulated data are generated and pre distorted based on the LUT generated in the previous step. The LUT only needs to be updated if the supply voltages or the carrier frequency is changed. The control signals are uploaded to the parallel data generator which sends them to the chip. The output of the chip is a modulated signal whose ACPR can then be measured. This type of pre-distortion measurement is a dynamic pre-distortion measurement technique instead of a static sweep. This is better than a static sweep as it can take into account any dynamic effect by using a high bandwidth signal for the purpose of non-linearity measurement.

Chapter 3 Design of the mixed-signal RF PWM

The primary focus of the design that will be presented here was to implement the digital to time conversion needed for the realization of an outphasing RF Pulse Width modulator in the mixed-signal domain. The complete block diagram of the designed and fabricated modulator is shown in Figure 18. The mixed-signal modulator is primarily consisted of two outphasing phase modulation paths where analog phase shifting of an existing sine wave in carrier frequency and according to the sampled and held in carrier frequency digital phase data takes place. The two phase-modulated sine waves are subsequently converted into digital square pulses and then are mixed using a CMOS AND gate in order to produce digital PWM pulses in the modulator output with phase that is connected with the phase information of the baseband signal and width that is related with the amplitude information of the baseband signal. The PWM pulses are finally driven to a 50-ohm load.

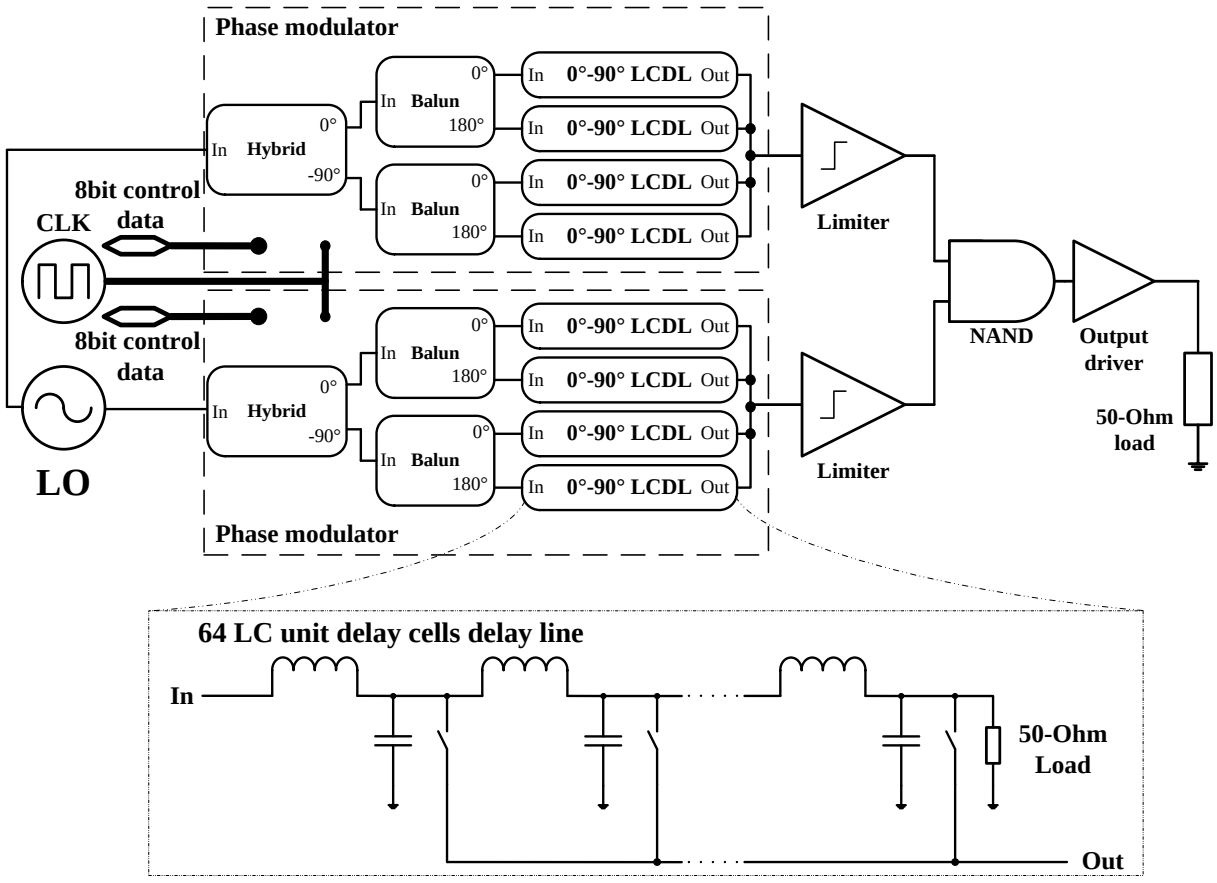

Figure 18 Block diagram of the complete mixed-signal RF PWM modulator

Shown in Figure 18, each phase modulation path comprises four analog LC delay lines (LCDL) each covering a 0o-90o phase shift range. The coarse phase shift to all four quadrants is continuously provided by the combination of an integrated hybrid LC Lange Coupler and two integrated baluns, shown in Figure 18.

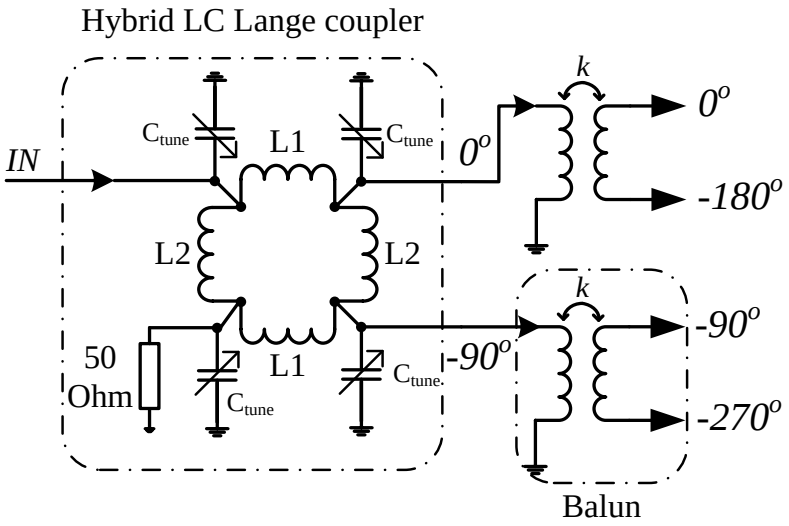

Figure 19 LO phase quadrant generation

Each LC delay line (LCDL) is implemented as tapped LC unit delay blocks connected in cascade so as to follow the distributed transmission line model. Depicted in Figure 19, phase selection in each LC unit delay block is implemented with nMOS transistors acting as switches. The outputs of all the tapping switches of the four LC delay lines in each outphasing path are shorted realizing a one-hot and single-level phase multiplexing scheme through a current summation common node.

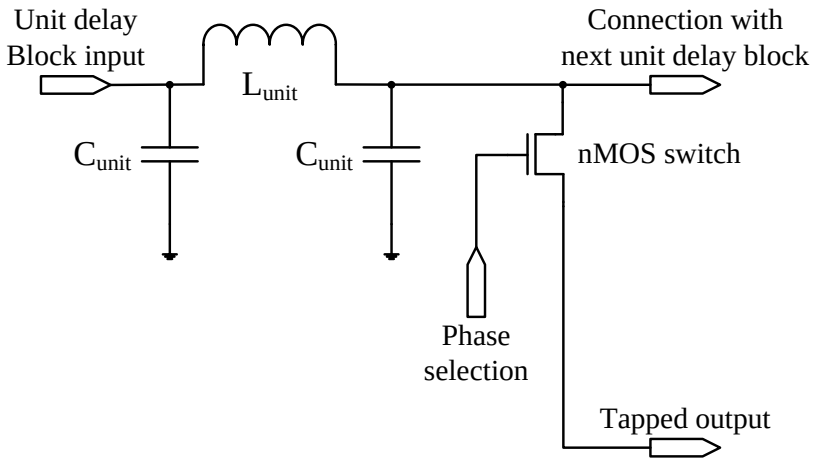

Figure 20 LC unit delay block

In order to minimize the wiring parasitics in the output common node of each phase modulator and optimize the dynamic behaviour of the modulator a “hair pin” layout structure for the integrated inductor is used in each LC unit delay block. As illustrated in Figure 20. This minimizes the inductor’s footprint around X-axis. In this way, compact LC delay lines have been realized that achieve a time resolution below 2 ps. Moreover, the attained time resolution is process-voltage-temperature (PVT) variation resilient due to the passive nature of the analog delay lines. Also a very small amount of power due to the small amplitude sine wave is consumed only on the termination resistors in each delay line and not inside the inductor chain.

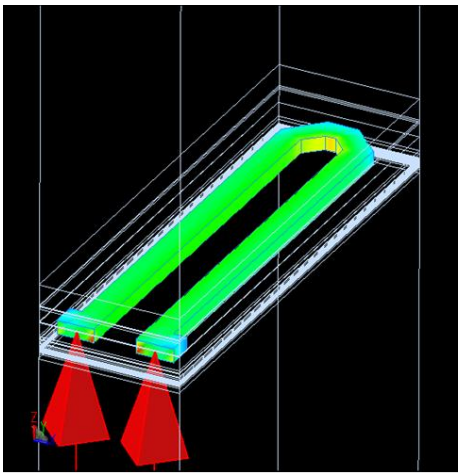

Figure 21 “Hair pin” integrated inductor layout

Regarding the operation of each of the two phase modulators, at each carrier period one phase of the sine wave carrier is selected synchronously. A differential clock and retiming D flip flops are used for synchronizing and sampling and holding the phase control data at carrier frequency. Also 8-bit decoders are employed for decoding the binary 8-bit phase control input to a one-hot representation of 2^8 bits for each outphasing path. There are 4x64 LC unit delay blocks per outphasing path in total.

The output of each phase modulator is a small amplitude sinusoid with amplitude in the order of 10-20 mVpp. The conversion of the two phase modulated sine waves into digital waves that maintain the phase information is accomplished with a chain of analog and digital limiting cells in each outphasing path, as depicted in Figure 21. Specifically, an analog limiting amplifier attains the gradual amplification of the small amplitude input sine wave into saturated levels. Then a digital level shifter and a tapped inverter chain drive the digital pulses onto a symmetrical CMOS NAND gate.

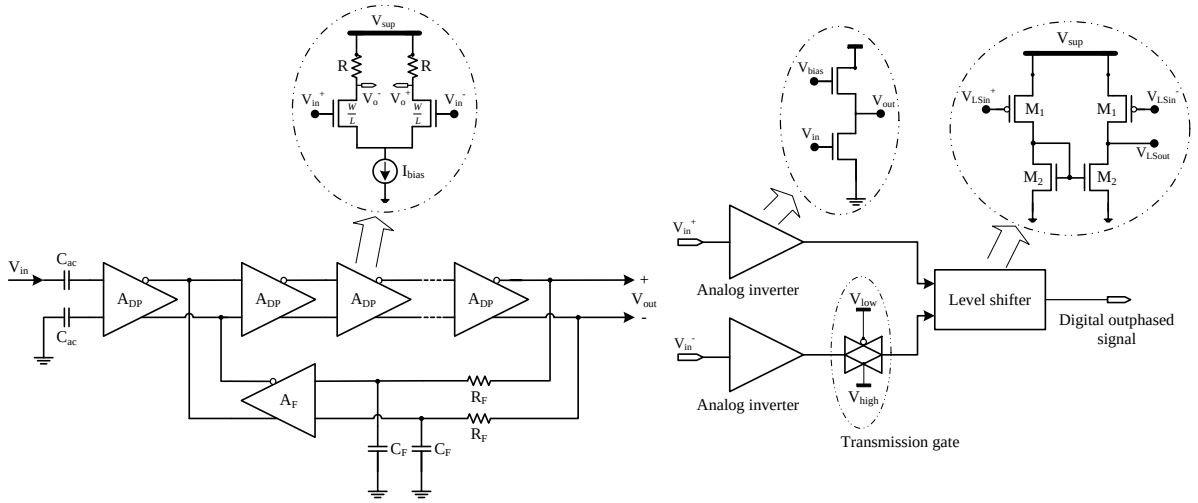

Figure 22 Analog limiting amplifier and analog to digital wave conversion

The digital mixing of the two outphased digital signals is implemented with a symmetrical and inherently fast and power efficient CMOS NAND gate shown in Figure 21. In order to minimize the pulse swallowing and pulse shrinking/extensioning effects in the output of the modulator, the NAND gate is as fast as possible driven by digital inverters with high driving capability. Also the output driver is implemented as a single digital inverter with capability to drive PWM pulses with minimum width onto a 50-Ohm load.

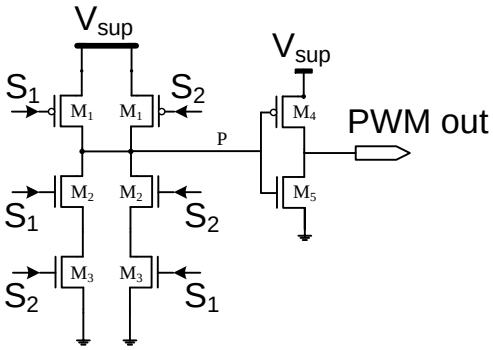

Figure 23 NAND gate and output driver

The complete chip layout of the designed mixed-signal RF Pulse Width Modulator that is developed in 40nm CMOS process is shown in Figure 23. The IC has symmetry around X-axis due to its outphasing topology. The outphasing phase modulators are placed up and down mirrored to each other and the remaining circuitry including the two limiting blocks, the NAND gate and the output driver is located at the middle of the chip. The I/O circuitry for the phase control data and the RF clock that is consisted of LVDS receivers is located along the top and bottom edges of the IC for the phase data and in the middle of the IC for the clock.

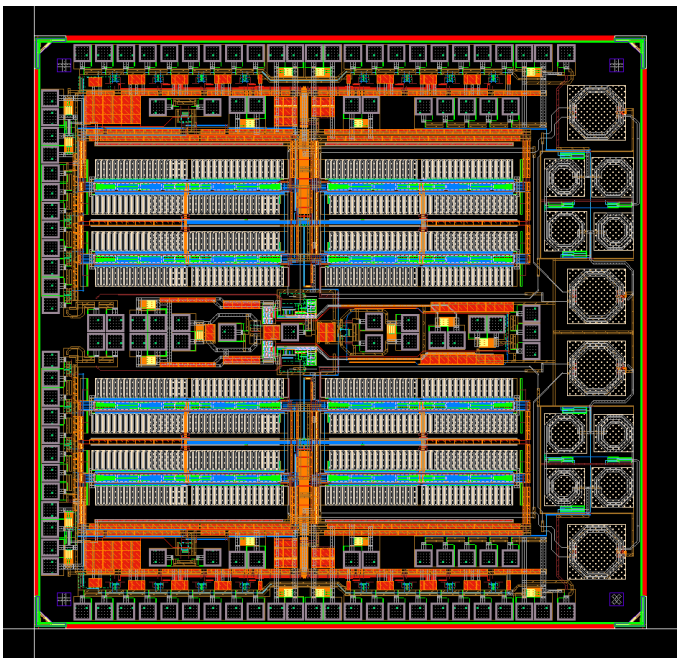

Figure 24 Modulator IC layout view

In order to validate the correct operation of the phase multiplexing scheme and specifically the operation of the D flip-flops that drive the tapping switches in the delay lines, I/O test signals which are separate inputs for the decoder and the digital control circuitry are used. The LVDS transceivers for these test signals are located along the left edge of the IC.

3.1 Test design for the evaluation of the mixed-signal RF Pulse Width Modulator

The overall test setup for the evaluation of the performance of the mixed-signal RF-PWM chip is shown in Figure 24. The digital phase data that are input to the modulator are first produced in a host-pc using MATLAB software and then are stored in multiple memory blocks of a Virtex-7 FPGA VC7215. Finally, together with the RF clock, they are phase-aligned and delivered through multi-gigabit transceivers to the modulator chip (DUT).

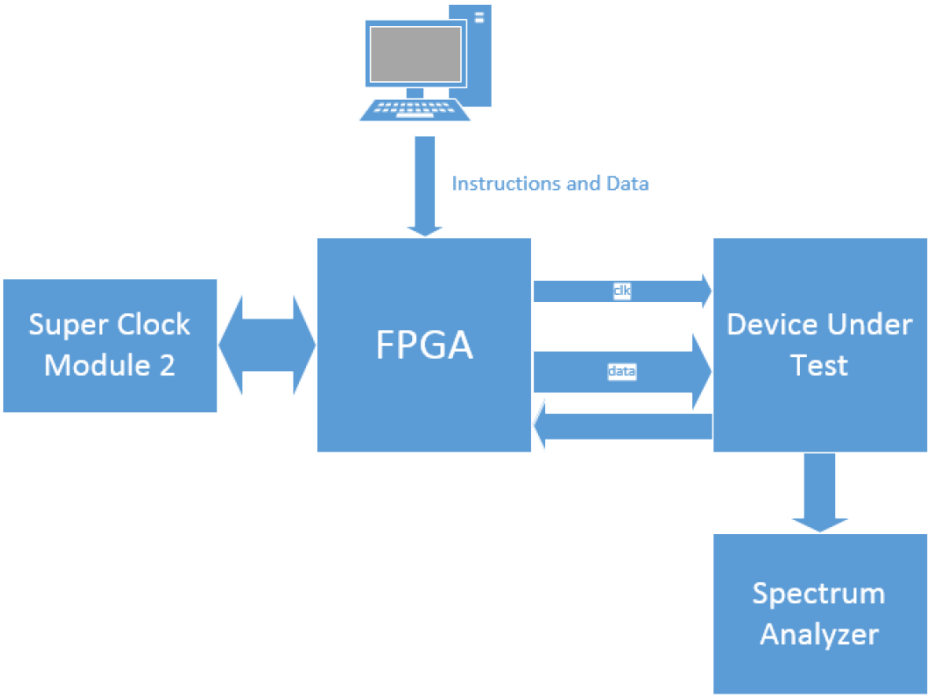

Figure 25 Overall test setup for mixed-signal RF-PWM modulator

The modulator has an 8-bit differential data input for each outphasing path. By including the test input and output bits in test operation mode, which are 4 per outphasing path, or the differential RF clock for the phase modulators in normal operation mode, a total of 24 FPGA transceivers are used. In order to have sufficient jitter margin for the high-speed FPGA-to-DUT transmission interface it is necessary that the common differential reference clock feeds the PLLs of maximum 12 transceivers. As a result, two phase-aligned external reference clocks are used for the 24 FPGA transceivers, which are produced by the SuperClock-2 module that is included in the FPGA development board.

As is illustrated in Figure 25, a reference oscillator is used as reference for two signal generators in order to get a sinusoid in carrier frequency (2.65 GHz) and also an external reference clock for the FPGA. The modulator ASIC has a sinusoid in carrier frequency and a differential clock in carrier frequency as carrier inputs. These two signals need to have as minimum skew as possible between them and the FPGA can address this issue by shifting independently the phase of the RF clock. Moreover, phase-alignment is also provided for the FPGA data differential outputs.

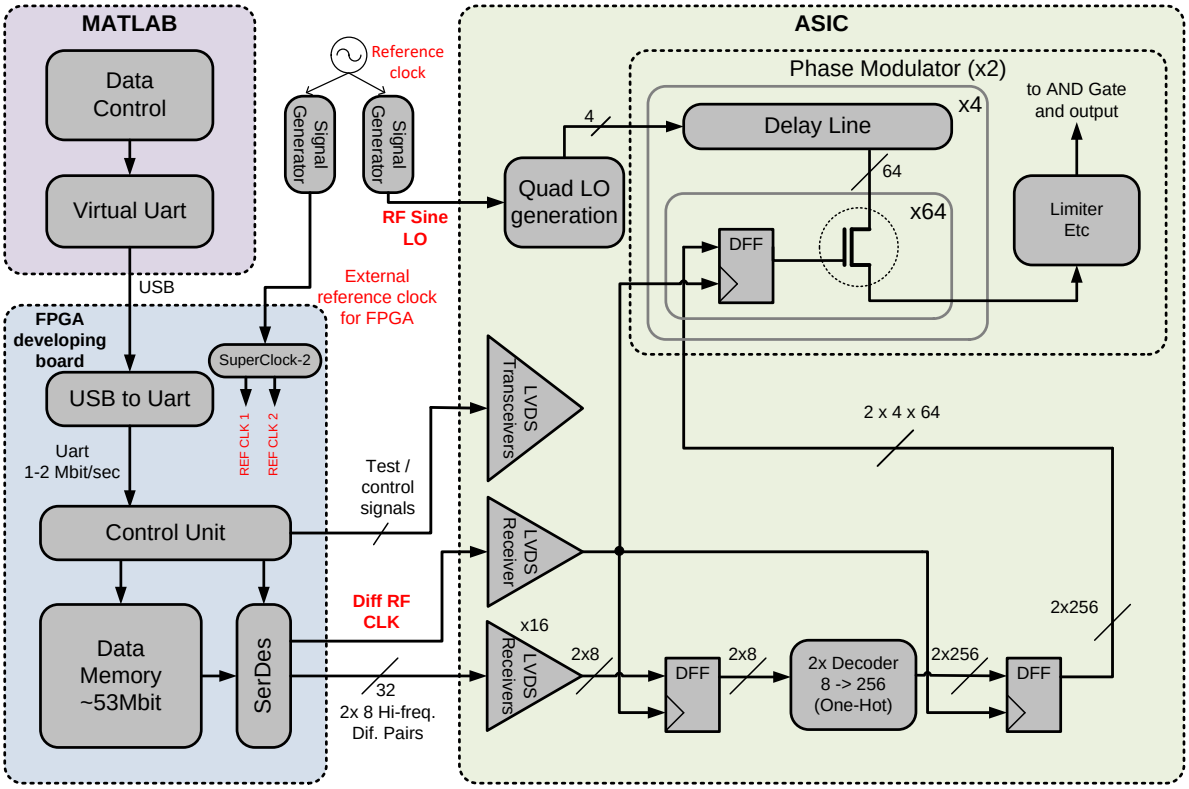

Figure 26 Detailed overview of the test setup including clock and sinusoid LO generation, data generation in MATLAB, the FPGA development board for the transmission of the data and RF clock to the modulator ASIC and the ASIC itself

Regarding the operation of the whole test setup, it operates in two modes: normal mode and test mode. The ASIC gets in test mode for debugging purposes through the use of a test enable signal and then the FPGA transmits a test data pattern which enters the chain of D flip-flops inside the phase modulators while receiving data from the chain scanning. In normal operation mode, data are sent from the computer (MATLAB software) to the FPGA where they are reproduced in a cyclic mode and then fed to the ASIC together with the RF clock through the multi-gigabit transceivers while being phase-aligned with one another and with the RF clock as well.

Chapter 4 Conclusion

Two chips and their test setups have been described in detail. Each of them is based on a different implementation of the same outphasing principle. The full digital implementation targets to a low area flexible implementation. As the digital implementation does not have on chip passives, it can be operated at a wide range of carrier frequencies. The Mixed Signal design targets to low power consumption by eliminating a lot of active components from the signal path. It is also able to operate at a higher carrier frequency due to its analog nature. Two proof of concept chips have been described in this deliverable. The circuits might look digital in nature but the design process they went through was far from a digital design flow. Each and every transistor in the asynchronous part of the circuit was manually laid out and sometimes the use of triple well transistors was made to protect the critical parts of the circuit from substrate noise. The chips were made through a full custom design flow. None of the traditional digital design techniques like timing closure etc. were used. Instead extensive simulation at circuit of individual blocks with parasitic extraction was done to ensure proper timing. It can be rightly said that the transistor level design and layout was more analog in nature than digital. Decoupling capacitors were placed on chip as close as possible to the critical asynchronous blocks. The ground and supply routing of all the blocks was kept separate to minimize supply noise interference. A ground reference was provided just near the bond pads. The total area for the digital chip is 3.3 mm x 1mm due to the bond pads. The core chip area is 700um by 800 um. Measurement results have been detailed in D4.3.

Chapter 5 List of Abbreviations

PCB	Printed Circuit Board
PA	Power Amplifier
IC	Integrated Circuit
RF PWM	Radio-Frequency Pulse-Width Modulation
Peak to Average Power Ratio	PAPR
ps	Pico second
LSB	Least Significant Bit
LUT	Look-up-Table